NEW CARBON-SILICON CARBIDE COMPOSITE BOARD MATERIAL FOR HIGH DENSITY AND HIGH RELIABILITY PACKAGING

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NEW CARBON-SILICON CARBIDE COMPOSITE BOARD MATERIAL FOR HIGH DENSITY AND HIGH RELIABILITY PACKAGING

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

Next-generation high-density packaging applications would necessitate a new base substrate material to achieve ultra-fine pitch solder-joint reliability and multiple layers of fine-line wiring at low cost. The NEMI 2000 roadmap defines the need for 4-8 layers of 5-10 μm wiring for future system boards. Microvia substrate technologies will play a crucial role in the printed wiring board (PWB) industry to accommodate these high performance requirements. The 2003 ITRS roadmap calls for organic substrates with less than 100-μm area-array pitch in the package or board by year 2010. Solder-joint reliability at such fine-pitch is a matter of concern for the industry. Use of underfills reduces thermal stresses but increases cost and, in addition, their dispensing becomes increasingly more complicated with the shorter gaps required for future interconnects. Therefore, there is a pronounced need to evaluate board materials with CTE close to that of Si for reliable flip-chip on board without underfill. Current substrates either do not conform to the stringent thermomechanical requirements (organic boards) of these future high-density packages or are uneconomical (conventional ceramic substrates).

Recently, a novel manufacturing process (using polymeric precursor) has been demonstrated to yield boards that have the advantages of organic boards in terms of large-area processability and machinability at potentially low-cost while retaining the high stiffness (~250 GPa) and Si-matched CTE (~2.5 ppm/°C) of ceramics. This work reports the evaluation of novel SiC-based ceramic composite board material for ultra-fine pitch solder-joint reliability without underfill and multilayer support. A combination of

numerical models and experimental analysis is used to evaluate thermomechanical reliability of test structures fabricated with C-SiC.

FE models were generated to model the behavior of flip-chips assembled without underfill and subjected to accelerated thermal cycling. These models were used to calculate solder-joint strains which have a strong direct influence on fatigue life of the solder. Multilayer structures were also simulated for thermal shock testing so as to assess via strains for microvia reliability. Via-pad misregistration was derived from the models and compared for different boards.

Experiments were done to assemble flip-chips on boards without underfill followed by thermal shock testing so as to get the number of cycles to failure. To assess microvia reliability, 2 layer structures containing vias of different diameters were fabricated and subjected to thermal cycling. Via-pad misalignment was also studied experimentally. Modeling and experimental results were corroborated so as to evaluate thermomechanical suitability of C-SiC for high-density packaging requirements.

Based on the results, it can be inferred that high board stiffness and low CTE (~ 3-4 ppm/°C) are needed to ensure reliability of high-density packages without the use of underfill. The test vehicle evaluation supported by modeling results indicate that the novel low-cost large-area processable ceramic matrix composite (C-SiC) has potential to be a promising candidate substrate material for next-generation microsystems.

CHAPTER 1

1. INTRODUCTION

This chapter begins with the description of trends in the microelectronics packaging industry which help to define the motivations of research for this work. Challenges that the industry is facing in order to be in line with these trends, using the currently available solutions, are then described. Candidates for base substrate material including boards with low coefficient of thermal expansion (CTE) are then discussed. The chapter then explains why Carbon-Silicon Carbide (C-SiC) composite is chosen to be investigated in this work followed by the description of its manufacturing process. Research objectives and thesis outline are then described to conclude the chapter.

1.1 Trends and Challenges

The increasing trend towards miniaturization and higher functionality in microsystems will drive greater demand for interconnect density at package and board levels. Two major components of future high density packaging are sequential build-up of multiple layers of conducting copper patterns with interlayer dielectrics on a board and multiple integrated circuits (ICs) flip-chipped on the top layer. A wide range of passives, wave-guides, and other radio frequency (RF) and opto-electronic components will be buried within the dielectric layers [1-3]. The interleaved copper and dielectric layers also

support the high density interconnects for power and signal requirements. The board material should therefore meet certain electrical, thermo-mechanical reliability, high density interconnect (HDI) processing, and cost requirements. Current substrates impose several fundamental barriers in meeting the reliability and stringent processability requirements of these convergent multifunctional microminiaturized systems. The increased functionality, wiring densities and reduced feature sizes necessitate novel substrate materials.

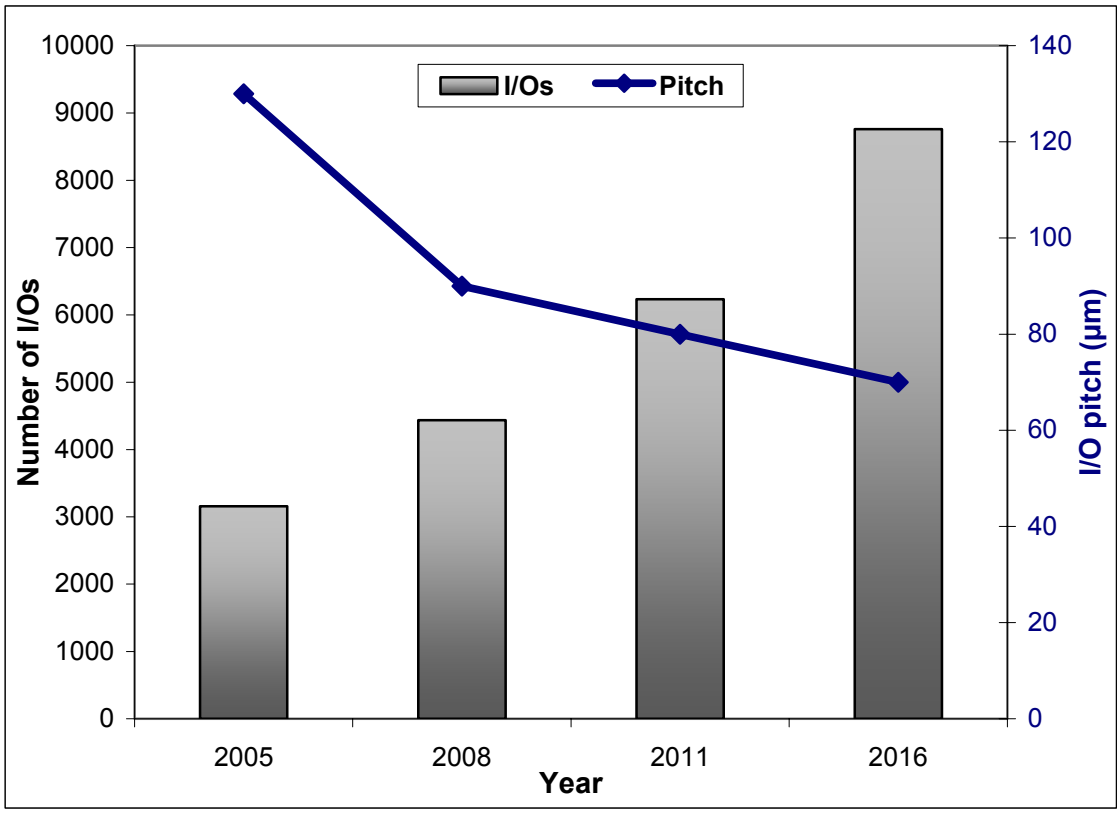
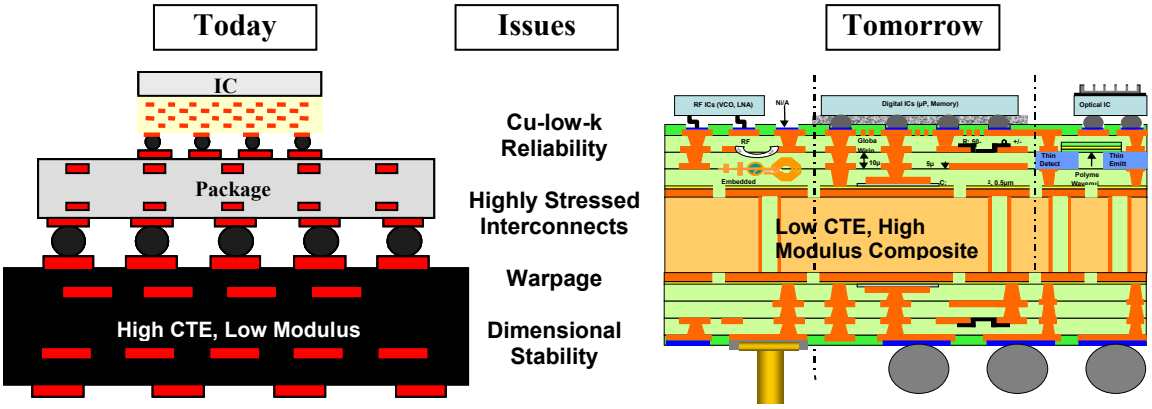


Figure 1: ITRS predictions number of I/Os and pitch for flip-chips.

1.1.1 High Wiring Density Challenge

International Technology Roadmap for Semiconductors (ITRS) [4] predicts that the number of input-outputs (I/Os) is expected to increase to more than 10,000 by 2016 as shown in Figure 1. The routing of future ICs with 10,000+ I/Os requires ultra fine feature sizes of at least 10µm lines/space widths and 35µm pad diameters [3, 5-6]. Furthermore, Sundaram *et al.* [6] had suggested that for an area array pitch of 100µm and lower, multilayer wiring of up to 10 signal layers with 10µm lines and spaces is necessary. The higher I/O count and density challenges of the Cu-low k devices upstream to the package level is driving the need to develop new packaging technology that can support the required number of layers to support high I/O count and I/O density packages as shown in Figure 2.



Lines (µm)	25-75		5-7
Vias (µm)	100		5-20
Capture Pads (µm)	400		5-20
Wiring (cm/cm^2)	300		10000
I/O (cm^{-2})	1000		20000
Pitch (µm)	200-300		20-50

Figure 2: Comparison of today's asymmetric and tomorrow's convergent high-performance microsystems.

The National Electronics Manufacturing Initiative (NEMI) [7] 2000 roadmap defines the need for 4-8 layers of 5-10μm wiring for future system boards. Microvia substrate technologies will play a crucial role in the printed wiring board (PWB) industry to accommodate these high performance requirements. The stringent need to process ten or more layers of thin films with via sizes of 10μm and capture pads less than 20μm requires layer-layer misregistration of less than 10μm over a 300mm substrate. This in-turn requires warpage control of 5-10μm per 25.4mm (1 inch) for a 0.65mm thick substrate [8]. The current organic based board materials are not suitable to meet these requirements as they lack dimensional control due to warpage and distortion during the sequential build-up process. Analytical modeling and experimental studies indicate that an ultra-high modulus (~350-450 GPa) [9] is required to meet the microvia/pad, line/spacing requirements. Moreover, the lack of dimensional stability and high warpage resulting from low stiffness (20-60 GPa) renders the organic boards unsuitable for emerging technologies like embedded actives, 3D packaging, buried die etc. [1-2]

1.1.2 Solder-Joint Reliability Challenge

The 2003 ITRS [4] roadmap calls for organic substrates with less than 100-μm area-array pitch in the package or board by year 2010 as shown in Figure 1. Reliability of an assembly is affected by the thermomechanical strains/stresses induced in the package due to the differences in thermal expansion coefficients among different components in the assembly under various thermal excursions. These thermomechanical stresses result

in low-cycle fatigue failure of solder joints, delamination of the solder bumps, and/or cracking of the build-up layers, leading to the failure of the assemblies. A silicon die has a CTE in the range of 2-3ppm/°C, while the conventional FR-4 substrate has a CTE in the range of 18-20 ppm/°C.

By employing underfills, thermal stresses at the solder bumps can be effectively reduced to improve the solder bump reliability. Nevertheless, underfill technology is costly and underfill dispensing becomes increasingly more complicated with the narrower and shorter gaps required for future interconnects. Usage of underfill is also known to cause the package to deform, leading to large peeling stresses at the die underfill and die-solder interfaces significantly impacting packaging reliability. Therefore, there is a compelling need to develop and evaluate cost-effective board materials with CTE close to that of Si for reliable assembly without the need for an underfill.

1.1.3 Microvia and Dielectric Reliability Challenge

Reliability of microvia interconnects is critical to the realization of high density package wiring. Although the new substrate materials with high modulus and low CTE can result in low warpage and eliminate the need for underfill, they can potentially cause delamination and cracking in the interlayer dielectric because of the high CTE mismatch between the dielectric and substrate. The ideal material and geometry for dielectric in conjunction with the substrate should lead to minimal interlayer stresses as suggested by Liu *et al.* [10]. The appropriate combination of electrical (low dielectric constant and low loss) and thermomechanical properties – low CTE, low stiffness, high toughness (elongation for failure) and thin film processability is not found in existing dielectric

materials. Therefore, appropriate thermomechanical simulations and reliability evaluation are essential to understand the material compatibility and failure mechanisms.

1.1.4 Cu-low-k Reliability Challenge

Cu-low-k structural integrity is another major reliability concern for high-density flip-chip packages. Interfacial delamination is commonly observed in low-k or ultra low-k interconnects after assembly due to large deformation and stresses generated by the thermal mismatch between the silicon die and the substrate. In the wafer back-end process, the crack driving force results from the thin film residual stresses within each layer and the thermal mismatch stresses within the low-k stacks. During the packaging process, in addition to the residual stresses and thermal mismatch stresses within the Cu-low-k stack, the global thermal mismatch between the package and IC exerts considerable external loads on the Cu-low-k structures. Compared with the oxide, the low-k dielectric is softer, expands more and adheres weakly to other materials. Since the adhesion strength for passivation / low-k dielectric interface is low, it is prone to delamination. While this indicates that interfacial delamination is not a critical issue for a standalone die, the problem is commonly observed in Cu-low-k interconnects after assembling the die into a flip-chip package as reported by Mercado *et al.* [11] and Du *et al.* [12]. The ITRS [4] 2003 has identified the UBM integrity and package compatibility as the key areas of challenge in the Cu-low-k IC assembly and packaging. Eliminating the global CTE mismatch between the package and the IC can minimize the Cu-low-k reliability problem by significantly reducing the interfacial stresses in the Cu-low-k stack

[11-13]. Therefore, a substrate with CTE close to that of Si is needed to eliminate external loads on Cu-low-k structures.

1.2 Why C-SiC?

1.2.1 Candidate materials

Many candidate materials explored to date possess a few attractive properties but none of them can satisfy all the proposed requirements for a next generation board. For example, pitch carbon (with diamond-like stiffness)-epoxy composite can yield a stiffness of 200 GPa when the reinforcement is more than 60 vol. %, however, resulting in a non-planar, brittle composite material. Metal matrix composites possess many attractive properties such as machinability, reasonably high stiffness and high thermal conductivity etc. However, achieving CTE less than 6 ppm/C with Al-matrix composites is a major processing challenge. Commercially available Al matrix composites filled with carbon cloth reinforcement do not possess attractive stiffness. Invar and other alloy based low-CTE boards have high density and very low stiffness as shown in Table 1. Ceramics like AlN and SiC possess the required stiffness and CTE close to Si to provide reliability without underfill but are very expensive (Table 1). More importantly, they are not available in large-area and need expensive processing. Table 1 lists the commercially available base substrate materials and C-SiC along with their thermomechanical properties, large-area fabrication capability and cost.

Table 1: Candidate materials for base substrate

Board	Supplier	CTE (ppm/°C)		Modulus (GPa)	Panel Area (in. x in.)	Cost ($)
		X/Y	Z			
FR-4		16-18	50	20-25	24 x 36	1-3 /sq.ft.
BT		17-18	64	~19.5		2-5 /sq.ft.
Arlon 45N	Arlon	14-16	55	~19	36 x 48	5-12 /sq.ft.
Rogers 4350	Rogers Corp.	14-16	50	11	24 x 36	7-16 /sq.ft.
GETEK	Polyclad	12-13	55	~1	36 x 48	2.5-7 /sq.ft.
Rogers 4003	Rogers Corp.	11-14	46	27	24 x 36	8-18 /sq.ft.
Cu-In-Cu	EIT	10-12		~1	13 x 19	0.6-0.7 /sq.in.
N4000-13SI	Park Nelco	9-13	55	28.5	12 x 18	3-7 /sq.ft.
MCL-E-679LD	Hitachi	8-11		27-30	18 x 24	3-5 /sq.ft.
Aramid-Epoxy	Dupont	7-9	50	14	24 x 36	8-16 /sq.ft.
Al_2O_3 ADS995	CoorsTek	7-8.3		54	4.5 x 4.5	8.5 /sq.in.
AlN AN215	Kyocera	4-5		320	4 x 4	7-10 /sq.in.
C-SiC	**Starfire**	**2-3**	**4.5**	**350**	**12 x 12**	**0.1-0.2/sq.in.**
High CTE		Medium CTE		Low CTE		

The Packaging Research Center at Georgia Tech has been evaluating various low CTE and medium CTE board materials such as carbon-cyanate ester, Al/SiC, AlN vis-à-vis FR-4 [14] for multilayer build-up wiring and solder-joint reliability without underfill. Except for AlN which, as mentioned earlier (Table 1), is very expensive and not available

in large area panels, all the boards showed failures. These failures were either due to low (or moderate) stiffness of the low CTE boards or due to high CTE mismatch in case of FR-4.

The ideal material should not only have the physical properties of ceramics but also have the large-area and low-cost processing capabilities of organic boards. In addition, the boards should allow for easy and inexpensive machinability.

1.2.2 Low CTE boards

Low CTE base boards have been developed and evaluated for increased flip chip reliability by several industry and academic research groups. IBM's glass-ceramic modules can be tailored to have exact CTE match with Si and hence showed reliability without underfill [2]. Novel laminate materials have also been developed with advanced fillers such as kevlar-aramid (Table 1) having negative CTE, resulting in low net CTE [15-16]. Dupont's non-woven aramid reinforced laminate systems (Thermount^{TM} laminates and prepregs) have tunable in-plane CTEs that reduce the CTE mismatch between the semiconductors and the laminate substrate [16]. This results in reduced strain on solder joints during thermal cycling, creating a higher reliability packaging system. These materials also have highest laser drillability due to the absence of woven glass fiber reinforcement. Low CTE boards of metal core (invar) have also been found to have better thermomechanical reliability [17]. HyperBGA^{TM} laminates from Endicott Interconnect utilize thin Cu-Invar-Cu (Table 1) cores and multilayer PTFE dielectric and these low modulus thin laminates have demonstrated reliable flip chip assembly at 180-225μm pitch [18]. Epoxy based low CTE laminates (MCL-E-679F and 679LD) from

Hitachi Chemical (Table 1) have also been shown to have benefits for fine pitch flip chip and wafer level package assembly and reliability [18]. Compliant packaging technologies typically use stress buffers between Si and package to solve the CTE mismatch problem (ex. Tessera's Wide Area Vertical Expansion technology) [20]. The internal stress due to the CTE mismatch between the die and the substrate is minimized in this package because the compliant polymer and the flexible copper lead enable the relative die to package movement in x-y-z directions during the temperature cycling.

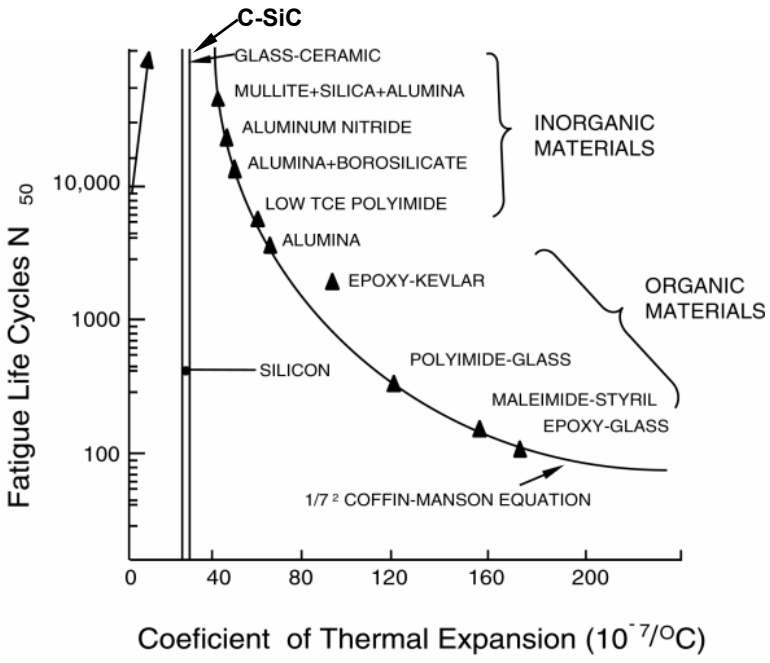


Figure 3: Solder joint fatigue life for different materials versus their thermal expansion coefficient [2].

However, none of these materials have the stiffness required for allowable low warpage and high-density wiring capabilities. Moreover, the CTE is also not Si-matched

and as the chip-to-package interconnect pitch is reduced from current to 150μm to future 20-50μm, the solder joint fatigue problem will increase and necessitate the use of package substrate/board materials with CTE in the 3-5ppm/C range close to Silicon. Figure 3 shows the fatigue life for various base-substrate materials versus their CTE. Though underfill materials are being used to enhance flip-chip reliability, they impose several bottlenecks to accomplish high component density, fine pitch and high I/O density. The CTE matched substrates have the real potential to meet flip chip reliability requirements without underfill materials.

New package or board materials with Si-matched CTE and ultra-high elastic modulus are therefore needed for the next generation of high-performance convergent microsystems to be able to fabricate ultra high-density wiring without big capture pads and to assemble area-array flip-chips with minimal stress on solder joint or perhaps completely eliminate underfills around the solder joint.

1.2.3 Proposed solution – C-SiC

A novel manufacturing process (patented [21] by Starfire Systems[1] Inc., NY) has been demonstrated to yield large-area thin carbon-silicon carbide (C-SiC) based composite boards with the required stiffness and Si-matched CTE at low cost. Unlike the conventional ceramic technology based on powder processing, this novel technology uses a polymeric precursor to derive the ceramic. This preceramic polymer allows design and fabrication of advanced ceramic matrix composites at low temperatures, in large area sheets with the required low CTE and high modulus. The properties obtained for C-SiC boards are shown in Table 2.

[1] Starfire Systems, Inc., 10 Hermes Road, Malta NY; http://www.starfiresystems.com

Table 2: Properties of C-SiC

Property	Current Values		Project Goal
	Set 1	Set 2	
Thickness (mm)	2	1	0.5 to 1
CTE (ppm/°C)	3	2.5	2-4
Modulus (GPa)	100	200	> 350
Flexure strength (MPa)	300	50	Panel cannot be brittle
Planarity (μm)	+/- 50	+/- 10	+/- 5
Panel Size (finished)	5" x 5"	5" x 5"	18" x 24"

Conventional ceramic manufacturing technology: The conventional technology for ceramic boards is limited to specialty materials that include AlN, Al_2O_3, and SiC ceramics. These boards are made via traditional ceramic manufacturing methods (like dinnerware) and are available in sizes up to 6 inches square. Typically these materials are over 0.125 inches thick. The cost of these boards is typically over $7.00/sq inch (Table 1). The small size of these relatively thick boards, combined with their cost, makes these boards suitable only for very limited specialty applications. Costs are driven by the high processing temperatures (typically over 2400ºC) and the associated capital equipment costs.

Ceramic from polymeric precursor: In this manufacturing route, typically the CMC materials are fabricated using layers of ceramic cloth or fabric laminated together with

the preceramic polymer resin to form large acreage structures. CMC structures 36 inches by 58 inches have been demonstrated. The combination of the polymer precursor with fibers, whiskers, and assorted powdered fillers allows for design and fabrication of advanced ceramic matrix composites with unique properties that cannot be manufactured by other conventional ceramic processing routes.

Polymer derived ceramic matrix composites (CMC) have been developed for both commercial and DoD (Department of Defense) applications. These structures exhibit high strength, stiffness, and dimensional stability for applications like turbine engine vanes, ceramic brake disks, aircraft exhaust ducts, and pistons for internal combustion engines. The cost, weight, and performance advantages of these advanced CMC materials is resulting in the displacement of traditional metals as automotive and aircraft manufacturers take advantage of the overall system benefits provided by the CMC components.

1.2.4 Fabrication of C-SiC Boards

The C-SiC boards were manufactured by Starfire Systems, Inc., and the process, described as a flowchart is shown in Figure 4. Composite panels of carbon fibers and a silicon carbide matrix are formed from commercially available carbon fiber fabrics and felts and a liquid polymeric ceramic precursor. The polymeric precursor is a highly branched polycarbosilane [21], which decomposes on firing to 850°C to give amorphous silicon carbide. Hydrogen is the main byproduct of the pyrolysis and is diluted and vented to the outside. In a typical preparation, layers of felt or fabric are cut to the desired size and shape, soaked in either the polymer or a slurry of polymer and silicon carbide

powder. Hot pressing using light pressure (60 - 300 psi) gives flat panels up to 10" x 10" square with porosities ranging from 20 to 50%. To improve strength and stiffness, the panels are re-infiltrated with the polycarbosilane and the pyrolysis repeated until the porosity is below 5% (8 to 10 cycles). Planarity is maintained by holding the panels flat under light pressure (1-5 psi) during these re-infiltration/pyrolysis cycles. To give the pore-free and planar surface required for fine-line wiring, the panels are lapped briefly and a paste of polycarbosilane/silicon carbide powder is worked into the surface. The panel is then pyrolyzed and given two polymer infiltration/pyrolysis cycles to insure a pore-free surface. The surface of the panels is finished with a light lapping and final polishing.

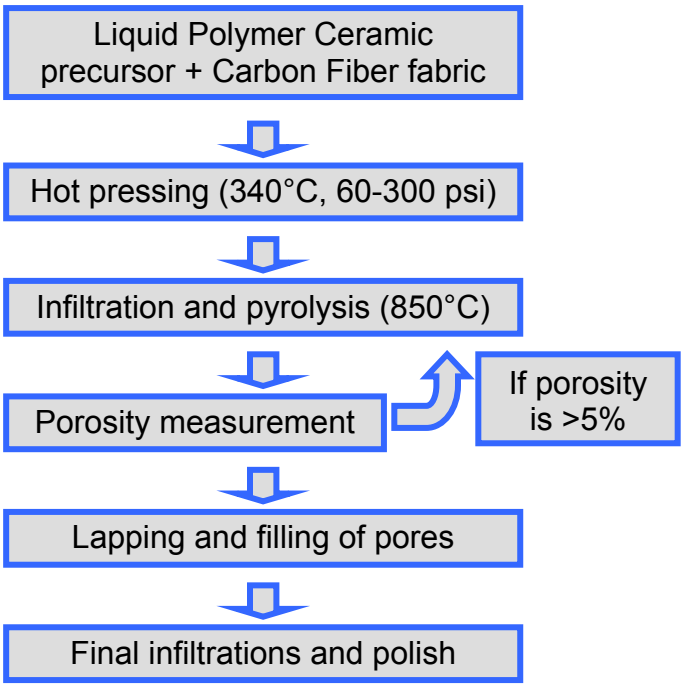


Figure 4: C-SiC Board Manufacture Process.

1.3 Research Objective

The objective of this research, guided by the trends and the challenges described above is to evaluate C-SiC board material using both Finite Element Analysis (FEA) and experimental analysis for high density and high reliability packaging. This includes formation of two-dimensional (2D) FE models of appropriate structures followed by application of corresponding processing conditions and/or thermal cycling. Experimental analysis includes the fabrication of test vehicles followed by reliability testing and measurements. Experimental results are then correlated with FEM results in order to analyze the suitability of C-SiC board material for future high-density microsystems packaging.

1.4 Thesis Outline

This work reports the thermomechanical reliability evaluation of the novel board material C-SiC for high density and high reliability microelectronic packaging. The board is evaluated for dielectric reliability, solder-joint reliability at 200μm pitch and 100μm pitch, microvia reliability for two metal layers and via-pad misalignment resulting from processing which are discussed in the subsequent chapters.

Chapter 2 deals with FE modeling and simulation of the test structures. It begins with illustration of the effect of substrate CTE and elastic modulus on structures. FE model formation for the dielectric reliability is then described. This is followed by solder-

joint reliability modeling for 200μm pitch and 100μm pitch. Microvia reliability and via-pad misregistration modeling is then described to conclude the chapter 2.

Chapter 3 describes the test-vehicle formation and the reliability tests that they are subjected to. Three different test-vehicles were fabricated for assessing solder-joint and dielectric reliability, microvia reliability and via-pad misalignment respectively. The test vehicles were evaluated by thermal shock testing except for via-pad misalignment which was obtained just after processing of structures.

Chapter 4 covers the results and discussion. It compares experimental results with FEM results. Appropriate discussion, based on results, is also presented in this chapter in order to reach conclusions which form the Chapter 5.

Chapter 6 suggests some of the areas in which future work can be carried out in order to further consolidate the results and explore the viability of C-SiC for next generation microsystems.

CHAPTER 2

2. FINITE ELEMENT MODELING AND PARAMETRIC ANALYSIS

Finite Element Models are developed to study the effect of substrate parameters on various failure mechanisms such as solder-joint fatigue, dielectric cracking and on factors that hinder high-density wiring such as warpage and via-pad misalignment. This chapter contains information on the geometric and material models used, applied boundary conditions and loads, and the parameters extracted in post-processing. The impact of solder-joint strains and warpage on reliability is explained in the beginning of the chapter. Four FE models, formed to evaluate different aspects of reliability, are then explained. These include Model 1 for showing the effect of substrate and evaluating dielectric and solder-joint reliability of 200μm flip-chip, Model 2 for evaluating solder-joint reliability of 100μm flip-chip, Model 3 for assessing microvia reliability and Model 4 for via-pad misregistration studies. FEM results revealing the effect of substrate CTE on solder-joint reliability and that of substrate modulus on warpage are presented in this chapter. All the other results of simulations are presented in Chapter 4 along with the experimental results to make a better case.

2.1 Effect of Substrate CTE and Modulus

Electronic packages undergo thermomechanical loading by repeated powering up and powering down of the devices [1-2]. To assess the effect of this thermomechanical

loading within a feasible time-frame, packages are subjected to accelerated thermal cycling, which usually includes exposing it to two extreme temperatures repeatedly within a short cycle time. Due to the difference in CTEs of different materials constituting an electronic package, they expand differently while being heated and contract differently while cooling. This differential expansion and contraction causes the package to experience thermomechanical strains, which depend on both the global and local CTE mismatch [22]. These strains (deformations) lead to induction of stresses in different constituents of a package depending upon their geometry, strength and modulus [23-24]. The following section describes the significance of solder-joint strains and warpage for high solder-joint reliability and high wiring density respectively. The effect of substrate CTE and modulus on the stresses, strains and deformations experienced by various entities constituting a package are then described based on FE simulations.

2.1.1 Solder-Joint Strains: Indicative of Solder Fatigue Life

The driving failure parameter used for fatigue life and hence reliability prediction of solder joint can be based on the solder strain range and the strain energy density parameters. These failure parameters can be seen as failure indicators for estimating the solder joint fatigue life. The strain range approach directly relates the normal or shear strain components induced in one thermal cycle to the fatigue life of the solder joint. When the solder joints deform due to cyclic loading, changes in displacements both in-plane and out-of plane from the center of the assembly, introduces normal and shear strains in the solder joints. This accumulated strain range per cycle weakens the solder joints and eventually leads to fatigue failure. The multi-axial stress and strain state

accumulated can be represented by the equivalent stress and equivalent strain components, which can be presented as equivalent elastic, plastic and creep strain components. The elastic part is very small compared to the inelastic solder strains. In FEM, the equivalent total strain, plastic and creep strain components are computed and used as failure parameter or indicators for fatigue analysis. For example, Doi *et al.* [25] used total strain range, while Frear *et al.* [26] and Gektin *et al.* [27] used total shear strain range as failure parameters. In other reports [28], plastic shear strain range was used to compute fatigue lives. The creep strain range per cycle [29] offers another failure parameter. The strain energy density has been used by some researchers [30-31]. The dissipated strain energy density per cycle may be regarded as a failure parameter for predicting fatigue damage. The relations reported in literature may use different parameters for failure criteria but all of them, in general, follow that lower the solder-joint strains, higher is the reliability and longer is the solder fatigue life.

2.1.2 Warpage: Indicative of Wiring Density

Warpage results from the mismatch in thermal expansion between the core board and the thin film build up materials. Building future discrete or convergent system boards for a typical electronic application requires at least 7-8 thin film build-up layers for signal and 3 layers for power distribution connected with vias [8-9]. This multiple layer build-up may lead to a situation of extensive warpage and via-pad misregistration as shown in Figure 5.

Figure 6 shows the scenario for current and future boards. Warpage and in-plane viscoelastic strains because of CTE mismatch in thin film build-up layers directly result

in in-plane distortion of the board. Warpage also limits the lithographic capabilities of the board by improper mask alignment and optics of the exposure. The consequences affect the design and fabrication of high-density wiring in two ways:

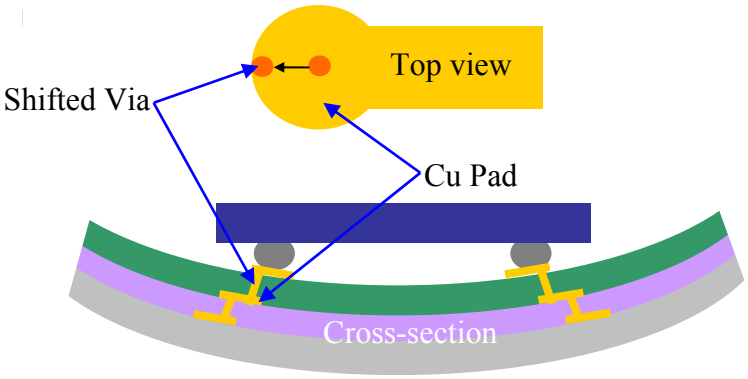


Figure 5: Via-pad misregistration resulting from warpage.

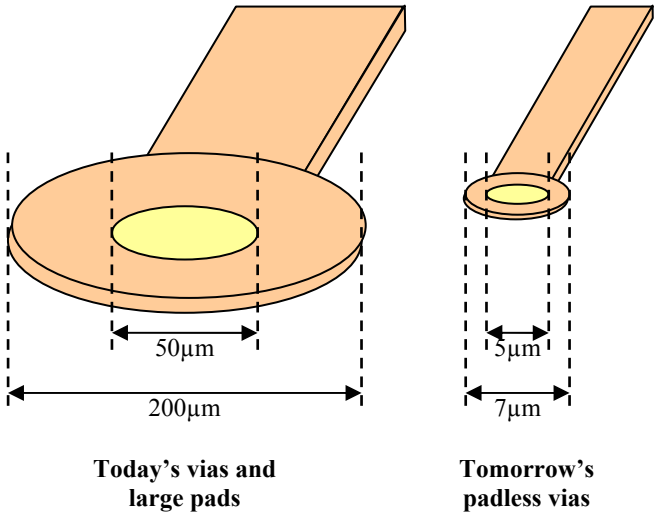


Figure 6: Today's versus tomorrow's capture pads and vias.

- *Via-pad misalignment*: The package designers incorporate the misregistration from layer to layer in a multilayered thin film structure with the help of large capture pads. For example, currently the pad size is typically four times the via dimensions in order to ensure the connectivity between different layers.
- *Minimum feature size*: High warpage prevents accurate definition of fine features. The designer can hence incorporate only coarser features.

Hence, warpage and dimensional change during build-up process can limit high-density wiring.

2.1.3 Effect of Substrate CTE and Modulus

To observe the effect of substrate CTE and modulus on solder joint strains and warpage, a fully parametric 2D half-symmetry FE model was constructed using ANSYS®. The parameters used for modeling are listed below:

1. Substrate width (for half symmetry)
2. Substrate thickness
3. Dielectric thickness
4. Solder mask thickness
5. Solder mask opening (for copper pad)
6. Copper pad bottom width (where it is in contact with dielectric)
7. Copper pad thickness
8. Copper pad top width (where it is in contact with solder ball)
9. Solder bump diameter
10. Stand-off height
11. Distance from neutral-axis
12. Die width (for half symmetry)
13. Die thickness

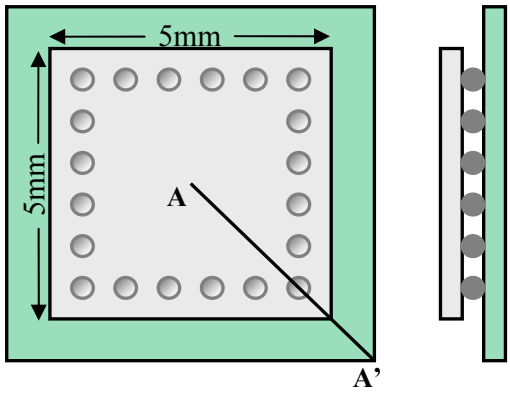


Figure 7: Schematic of a package showing AA' section used for FEM.

As the flip-chip being modeled has a peripheral row of solder bumps (Figure 7), when a 2D symmetric cross-section is taken, only a single solder bump needs to be incorporated into the model. Half-symmetry was applied along the diagonal so as to capture the solder furthest from the center of the package as shown in Figure 7. The FE model, as shown in Figure 8, is the cross-section of the package taken at AA' in Figure 7.

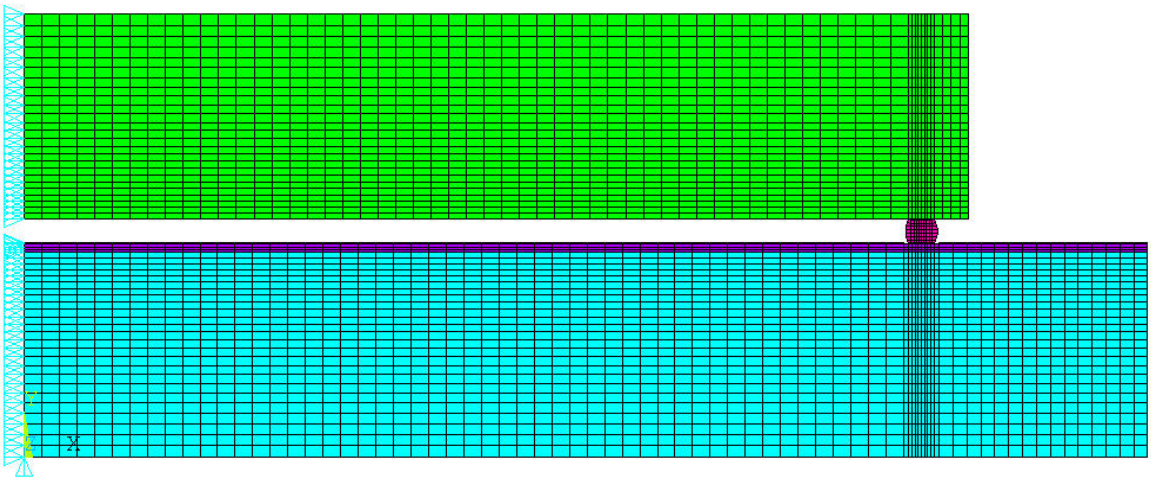


Figure 8: 2D Half-symmetry model formed for section AA' (Figure 7).

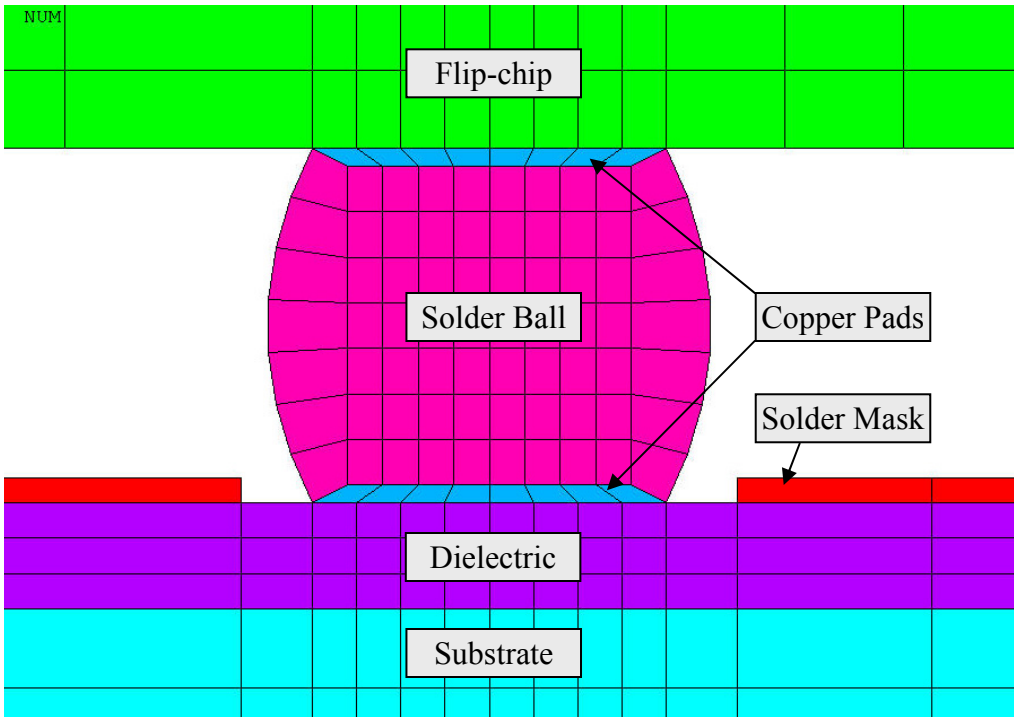


Figure 9: Enlarged view of meshed areas near the solder ball.

Figure 9 shows an enlarged view of the mesh near the solder ball. Since the areas near the solder bump are most critical [32-34] from reliability point of view, the areas near solder ball are finely meshed. Although the areas away from the solder ball are meshed coarsely, the aspect ratio of all the elements is maintained below 1:10 to facilitate better interpolation of results within an element. As can be seen from Figure 8 and Figure 9, the model consists a flip-chip assembled without underfill on a substrate having a dielectric layer, copper pad and solder mask layer. The geometry modeled is copper-pad defined and not solder-mask defined as shown in Figure 9. Table 3 shows the properties of various substrates, dielectrics and other materials studied in this work.

Table 3: Material properties used for FEM

Base Substrate Materials			
Material	Young's Modulus (GPa)	CTE (ppm/°C)	Poisson's ratio
FR4	24	16	0.15
C-SiC (1 / 2 / 3)	80 / 150 / 200	3	0.3
Dielectric Materials			
Material	Young's Modulus (GPa)/ Strength (MPa)	CTE (ppm/°C)	Poisson's ratio/ Cure Temp (°C)
Epoxy	3 / 30-83	65	0.4 / 135
BCB	2.9 / 87	50	0.4 / 250
Polyimide	2.5 / 200-390	15	0.4 / 190
PPE	2.4 / 71	13	0.4 / 175
Other Materials Properties			
Material	Young's Modulus (GPa)	CTE (ppm/°C)	Poisson's ratio
Silicon	130	2.7	0.28
Copper	104	17	0.34

The dimensions of different components of the package as used in FE modeling are listed in Table 4. The 2D plane-strain finite element model has symmetry boundary conditions applied along the left edge of the model. The left bottom corner node is additionally constrained in the vertical direction to prevent rigid body motion. The finite

element model is parametric and the various geometric and material parameters can be changed to study their effect on reliability. Table 5 lists the material models that were employed for FE simulations.

Table 4: Dimensions used for parametric FEM

Component	Dimension
Substrate Thickness	0.8mm
Dielectric Thickness	30µm
Solder Mask Thickness	7µm
Copper Pad Thickness	5µm
Solder Pitch	200µm
Solder Diameter	100µm
Die Thickness	0.8mm
Die Size	5mm x 5mm

Table 5: Material Models used for FEM

Material	Model
C-SiC	Linear Elastic with Orthotropic CTE
FR-4	Linear Elastic Orthotropic
Dielectric/ Solder Mask	Linear Elastic
Copper Pad	Bilinear Elastic-Plastic
Solder (Sn/Pb)	Temperature Dependent Multi-Linear Elastic Plastic
Die	Linear Elastic

The bilinear kinematic hardening behavior of copper as used for FE simulations is shown in Figure 10. Temperature dependent multi-linear elastic-plastic property of the solder ball (Sn/Pb) is illustrated in the Figure 11.

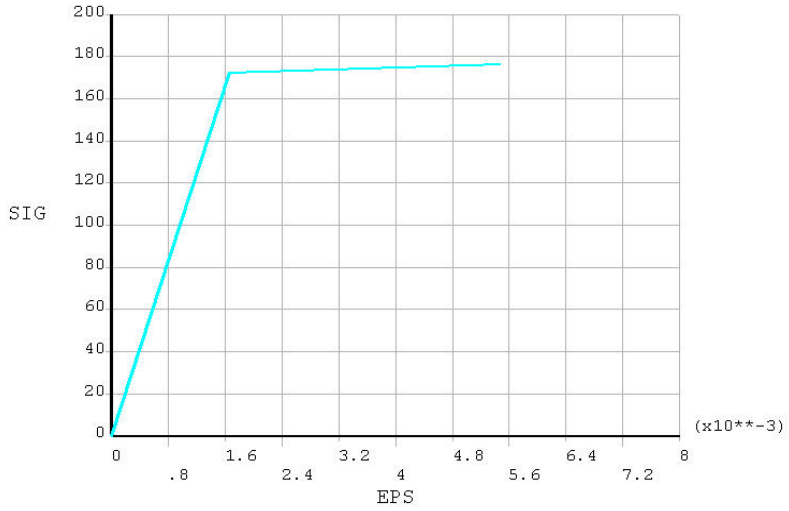


Figure 10: Bilinear kinematic hardening behavior of copper.

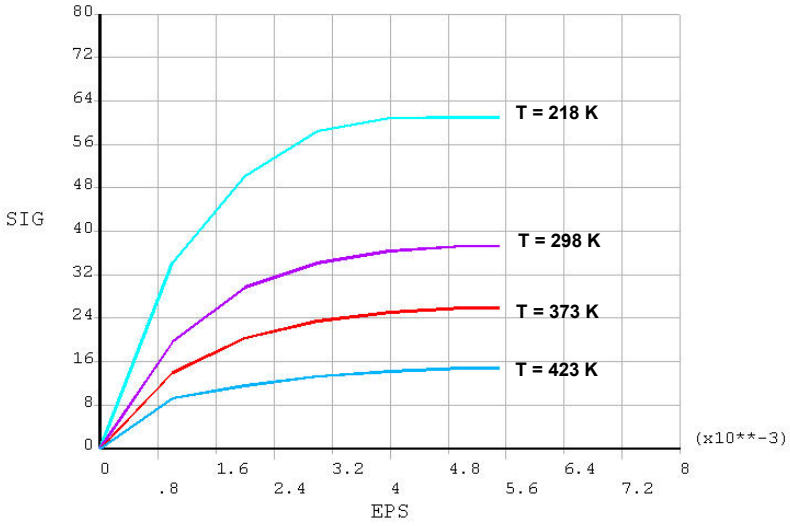


Figure 11: Temperature dependent multi-linear elastic-plastic behavior of Sn/Pb solder ball.

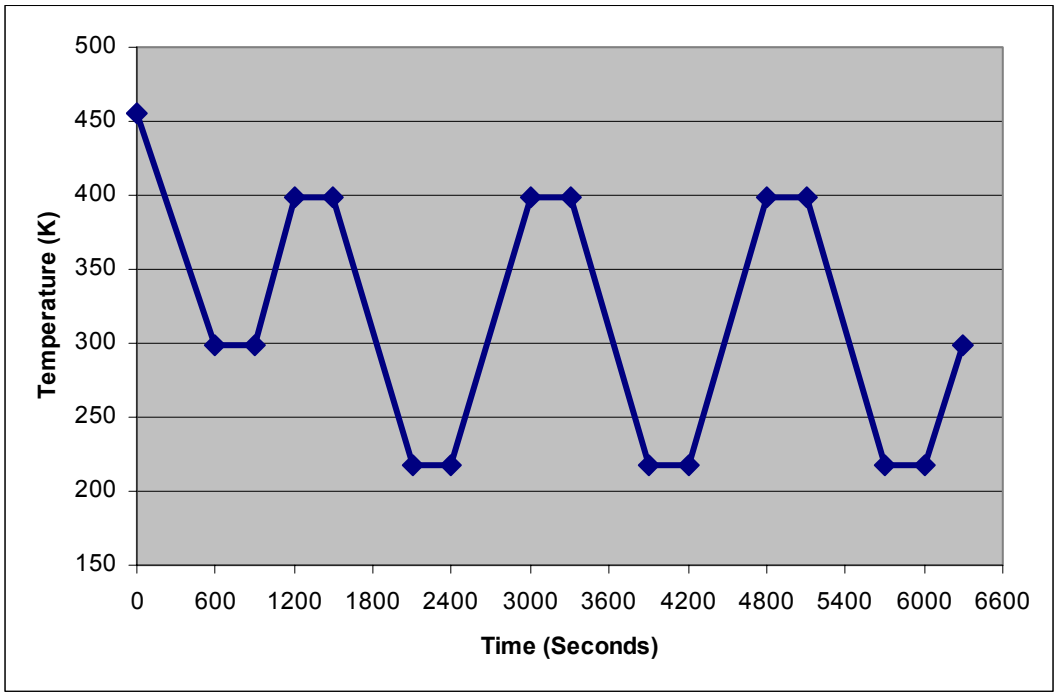


Figure 12: Simulated thermal cycle for calculating solder-joint strain.

In the simulations the assembly is first cooled down from the eutectic solder reflow-temperature of 183°C to room temperature (25°C) over a 10 minute period. Thermal shock simulation is done 5 minute high and low temperature dwells, and 10 minute transition time. Figure 12 shows the simulated thermal cycles. The high dwell temperature is 125°C and the low temperature dwell is -55°C. The stress free temperature is taken as 183°C and three thermal shock cycles are simulated to obtain stabilized values for the solder joint strain. A strip of elements is selected towards the die-side (because maximum strains were observed on the die side) as shown in Figure 13, and equivalent plastic strain is calculated as the area-weighted average of strains for these elements.

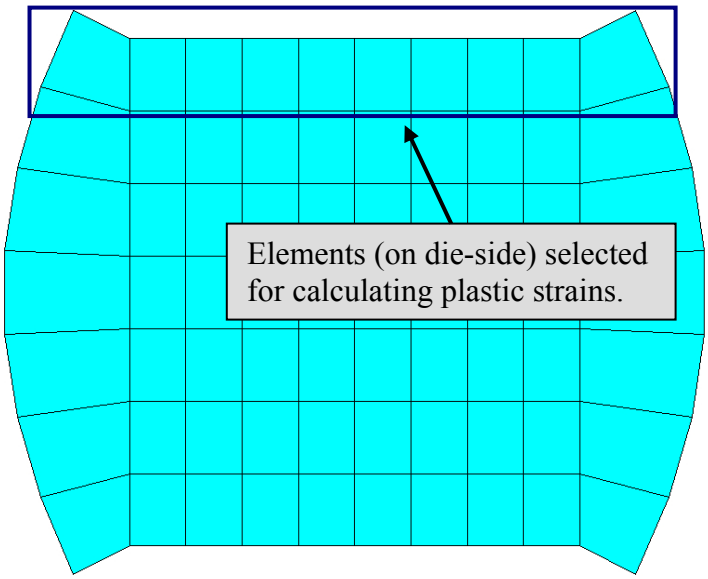


Figure 13: Strip of elements on die-side for calculating area-weighted average of equivalent plastic strains.

For assessing the effect of substrate CTE on the solder joint strains, which are a direct indicative of the solder-joint reliability, the modulus of the substrate was kept as 180GPa and the CTE was varied from 2.5ppm/°C to 7.5ppm/°C. Total von Mises solder-joint strains were obtained for each case and plotted as a function of substrate CTE as shown in Figure 14. Figure 14 clearly indicates that as the substrate CTE deviates from 2.6ppm/°C which is the CTE of the silicon flip-chip, the solder-joint strains increase abruptly. This increase in solder-joint strains if detrimental to the solder-joint reliability and reduces the fatigue life of the solder severely. Therefore, to ensure maximum reliability of solder-joints, substrate CTE must be as close to silicon CTE as possible.

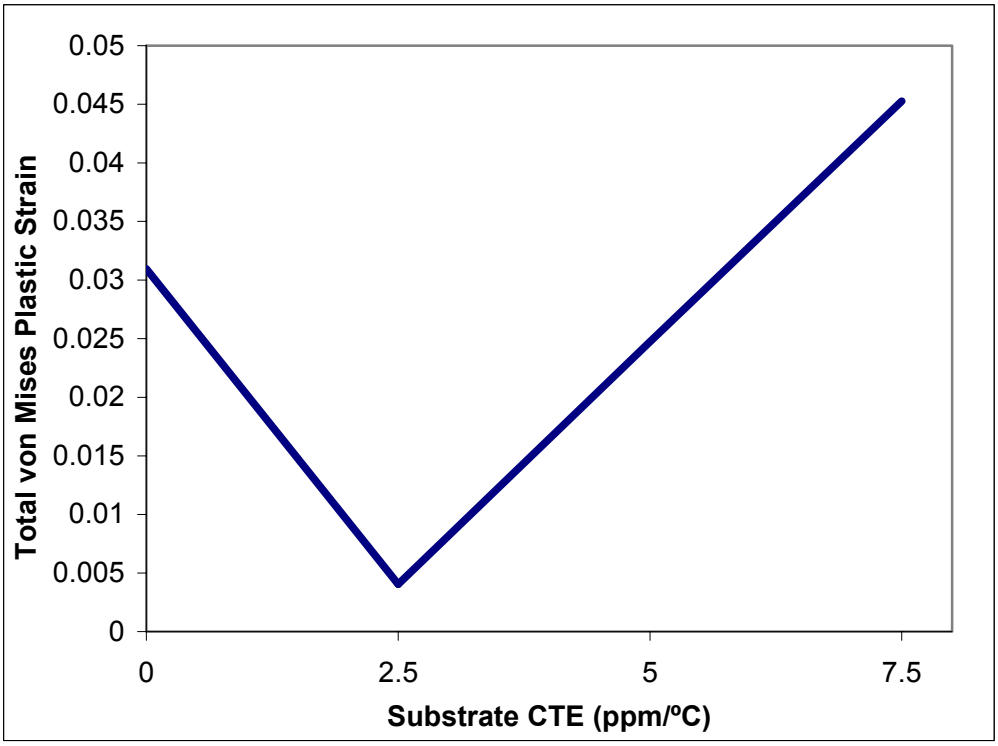


Figure 14: Solder-joint strain variation as a function of substrate CTE. (Dimensions used for modeling are given in Table 4)

To predict the effect of substrate modulus on the warpage the CTEs of the substrate was kept as 2.2ppm/°C and the modulus was varied from 10GPa to 180GPa. Warpage was obtained for each case and plotted as a function of substrate modulus as shown in Figure 15. It is evident from Figure 15 that as the substrate modulus increases the dimensional stability is enhanced resulting in low warpage values. Similar trends were observed by S. Banerji [8]. The results depicted in Figure 15 are obtained for a single layer build-up. The warpage, as suggested by Banerji *et al.* [9], increases as the film thickness is increased, leading to higher via-pad misalignment. Higher modulus is therefore desired to achieve high-wiring density. The in-plane strains will be discussed in Chapter 4.

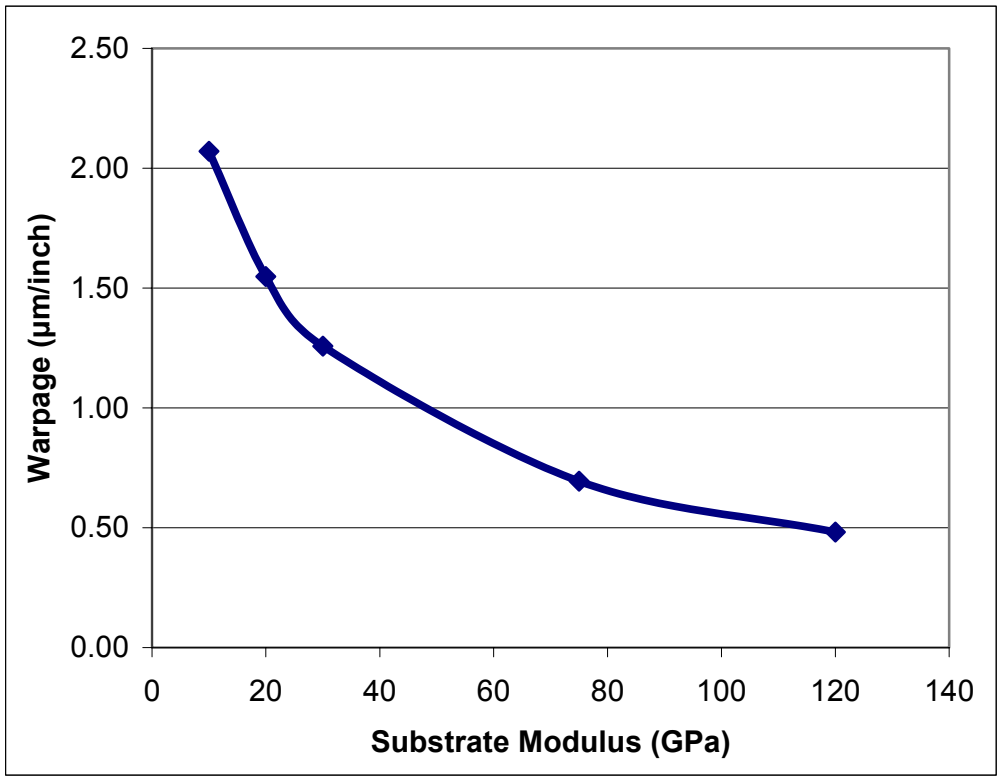


Figure 15: Warpage variation with substrate modulus. (Dimensions used for modeling are given in Table 4)

2.2 Thermomechanical Reliability

2.2.1 Dielectric Reliability

C-SiC, as shown in Table 2 has a CTE of ~2.2ppm/°C as opposed to conventional substrates like FR-4 (~17ppm/°C). This silicon matched CTE may result in an increased CTE mismatch between the substrate and the dielectric, particularly when conventional epoxy based dielectrics are used. Therefore, stress analysis in the dielectrics was done with FE modeling to understand the dielectric behavior for the build-ups on C-SiC. To

evaluate their influence on dielectric stresses, different dielectrics with different thicknesses were modeled.

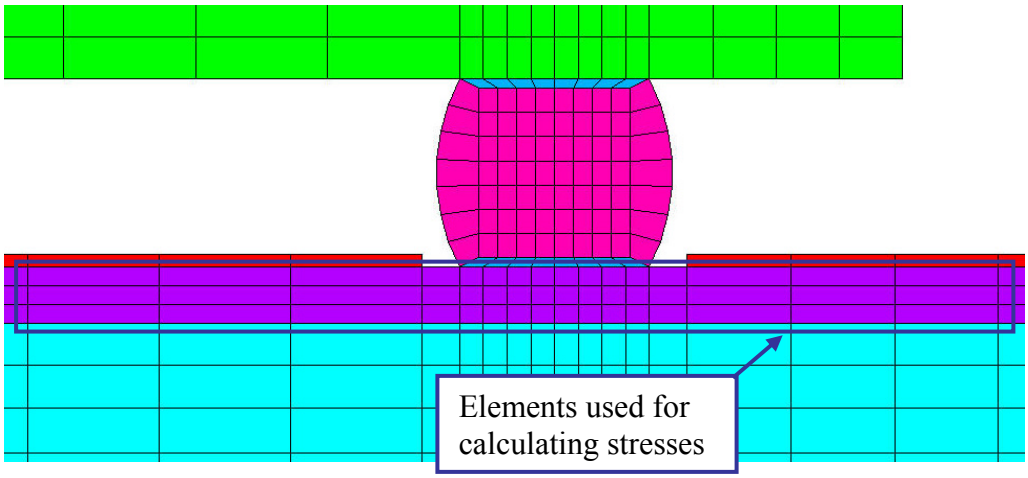


Figure 16: Elements near the copper pad used for calculating von Mises stresses.

For assessing the dielectric reliability, a similar model (Figure 7 and Figure 9) as for predicting the effect of substrate CTE and modulus was used. Monotonic cool down from the stress-free temperature (~183°C) to room temperature (~25°C) in 10 minutes was used as the thermal loading. The portion of dielectric near the copper pad was seen to be stressed the most and a fixed width on either side of copper pads, as shown in Figure 16, was chosen for calculating von Mises stress in the dielectric. This width was held constant for calculation of stresses in different build-ups. All the elements, contained in this width were selected and the values of stress for all the nodes of these elements were used for getting maximum, minimum and average stress. Three cases with different dielectrics of different thicknesses were simulated and compared for dielectric stress analysis. Table 6 lists the three cases that were modeled.

Table 6: Dielectrics and their dimensions modeled for dielectric stress analysis

Dielectric Material	CTE (ppm/°C)	Thickness (μm)
Epoxy	65	60
BCB	50	6
PPE	13	30

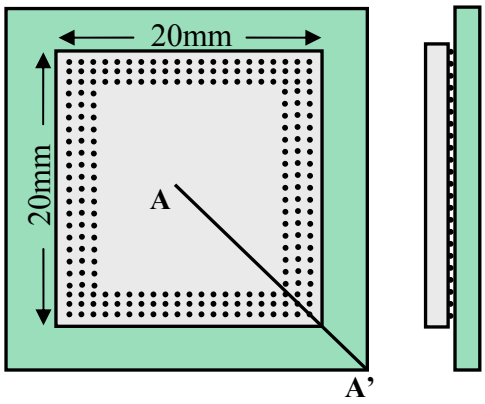


Figure 17: Schematic of a package with 3 rows of solders on peripheral flip-chip.

2.2.2 Solder-Joint Reliability

FE modeling was done to evaluate solder-joint reliability for different solder bump pitches, solder materials and die sizes. Two different configurations, one having only one solder bump row (Figure 7) and the other having three solder bump rows (Figure 17 and Figure 18) on the peripheral flip-chip were modeled.

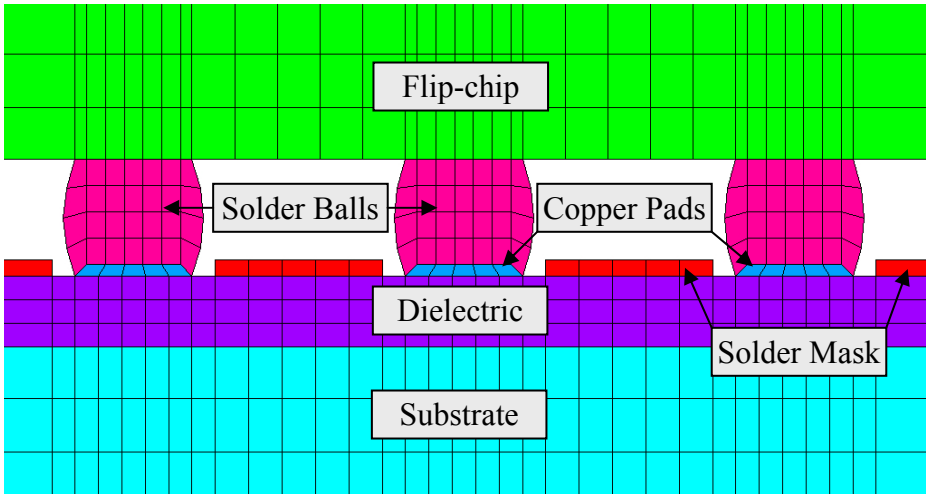


Figure 18: Mesh for 3 rows of solders on peripheral flip-chip.

Table 7: Cases studied for solder-joint reliability

Substrate	Solder Material	Solder Pitch (μm)	Die Size (mm x mm)	No. of rows of solders on peripheral flip-chip
C-SiC	Sn/Pb	50, 100 & 200	5 x 5	1
FR-4	Sn/Pb	200	5 x 5	1
C-SiC	Sn/Ag	200	5 x 5	1
C-SiC	Sn/Pb	50, 100 & 200	10 x 10	1
C-SiC	Sn/Pb	50, 100 & 200	20 x 20	1
C-SiC	Sn/Pb	100	20 x 20	3
C-SiC	Sn/Ag	100	20 x 20	3

Table 7 lists the various different cases modeled for solder-joint reliability. As mentioned earlier, the assembly was first cooled from the stress free temperature (183°C for Sn/Pb solder and 260°C for Sn/Ag solder) to the room temperature followed by three thermal cycles (Figure 12) to obtain stabilized cyclic results for the solder. Simulation results were compared for assembly with FR-4 and C-SiC as substrate.

There has been a constant push in the recent years for using lead-free solders owing to the toxic effects of lead. International laws have been formed to ban or reduce the use of lead in electronic products [35-37]. The most investigated solder systems are eutectics[2] of SnAg (Sn96.5% Ag3.5%), SnAgCu (Sn95.5% Ag3.5% Cu0.7%) and SnCu (Sn99.3% Cu0.7%). These material systems invariably have a melting point higher and are harder than that of the conventional SnPb (Sn63% Pb37%) solder system. Therefore, there have been extensive studies related to reliability of lead-free solders [38-44]. For the sake of comparison and to evaluate the performance of lead-free solders on C-SiC, modeling was also done taking SnAg as the solder material (Table 5).

Metals such as Au, Ag, Ni, and Cu dissolved in the solder change the phase evolution of both lead-free and tin-lead solder interconnects. They are present in small amounts as additives to the solder or are used as protective coatings (surface finish) on metallizations (pads). These metals diffuse so rapidly during reflow and thermal cycling that they are available in sufficient quantity at the solder/metallization interface or within the solder to facilitate the formation of intermetallics. This phenomenon has a great impact on thermomechanical reliability [45] especially in case of lead-free solders but for the sake of simplicity, it is not taken into account for modeling done in this work.

[2] A eutectic alloy is the lowest melting alloy for a given set of constituent metals. It forms at a particular composition of the constituents, known as eutectic composition.

2.3 High Wiring Density

2.3.1 Microvia Reliability

An axisymmetric model of a single microvia interconnect, as shown in Figure 19, was used assessing microvia reliability. The double-sided test structure is modeled with appropriate boundary conditions as can be seen from Figure 19.

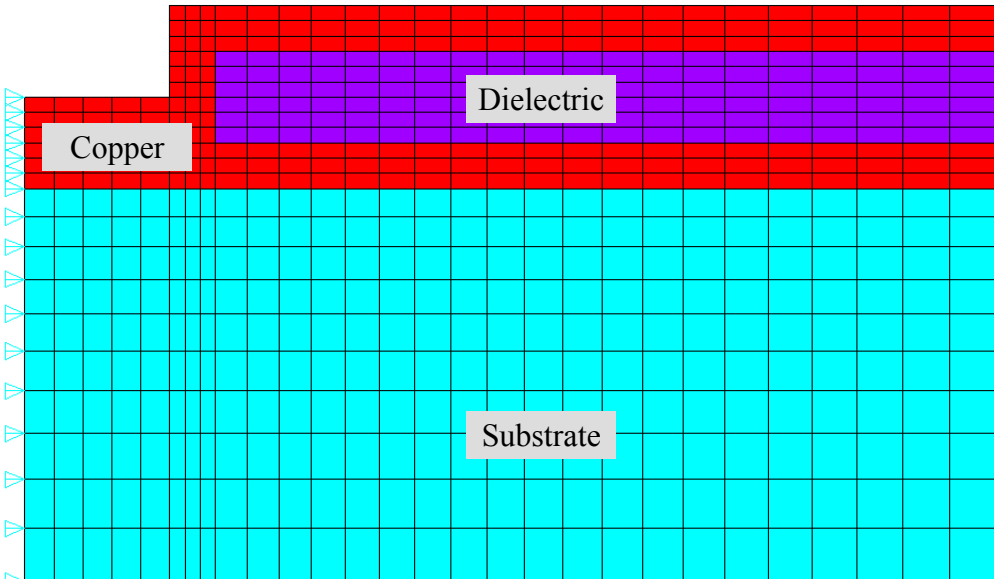


Figure 19: Axisymmetric model for evaluating microvia reliability.

The thermal profile for the simulation consisted of cooling the assembly from dielectric cure temperature to room temperature, one hour dwelling at room temperature followed by thermal shock cycling between -55°C to 125°C with 10 minutes dwell at extreme temperatures. The results were obtained for a stabilized cycle after 3 thermal

cycles. Simulations were done with different via diameters and dielectric materials so as to study their effect on via reliability and dielectric stresses. Table 8 and Table 9 list the dimensions of parameters used and cases studied for microvia reliability modeling respectively.

Table 8: Dimensions used for parametric FEM for microvia reliability

Component	**Dimension**
Substrate Thickness	0.8mm
Dielectric Thickness (both D1 & D2)	5µm
Copper Pad Thickness (both M1 & M2)	5µm
Pad Diameter	400µm

Table 9: Cases modeled for microvia reliability

Substrate	Dielectric Material	Via-Diameter
C-SiC	BCB	20, 25, 50 & 100
C-SiC	Epoxy	25
C-SiC	PI	25
FR-4	Epoxy	25

2.3.2 Warpage and Via-Pad Misalignment

A half-symmetry 2D FE model was formed to simulate the behavior of the base substrates (C-SiC and FR-4) when coated with BCB in order to measure via-pad misalignment induced during the curing process. The model consisted of 50μm diameter and 2 μm thick copper pads on the boards with BCB on top. Thickness of the BCB layer was 8 μm which was cooled from BCB curing temperature of 250°C to room temperature in different steps so as to imitate actual curing process. Effective via-pad misalignment was obtained by subtracting the values of displacement of the center of pads when cooled with and without BCB layer. Similar models were generated to simulate multiple layers of BCB to assess its effect on via-pad misalignment. Warpage induced due to curing of BCB layers was also computed using similar models and the results were extrapolated so as to compare with experimental results. Results were generated to show the warpage induced as a function of film thickness. Via-pad misregistration was computed and compared for 300mm x 300mm sized C-SiC and FR-4 boards with multiple layers of BCB.

2.4 Summary

Literature review suggests that there are different parameters being used in various fatigue life models for the failure of solder bumps. Nevertheless, almost all of them take into account solder-joint strains for estimating the fatigue life, indicating that solder-joint strains are the primary indicative of solder bump reliability.

Board warpage is a result of CTE difference in the materials constituting multi-layer build-up. Warpage may be quite extensive in certain cases leading to severe via-pad misalignment which compels designers to use large capture pads for vias to accommodate the misregistration ultimately leading to lower wiring density. Furthermore, warpage limits the lithographic definition of fine features on the board, hindering the goal of achieving high wiring density.

With the aim of evaluating solder-joint reliability and suitability of C-SiC boards for high wiring density, various FEM models were created. Different models were constructed to estimate dielectric reliability, solder-joint reliability (200µm and 100µm pitch), microvia reliability and via-pad misalignment. Model geometry, material models and loading conditions are described for each of the models. These models, as described in Chapter 4 are used to get solder-joint strains and warpage for C-SiC vis-à-vis FR-4.

CHAPTER 3

3. FABRICATION AND TESTING

This chapter contains the methodologies and process steps used for fabrication of test vehicles. Three types of test vehicles were fabricated with C-SiC to evaluate various reliability aspects of high-density packaging. Fabrication of test vehicles for solder-joint reliability (both 200µm and 100µm pitch) and dielectric reliability are first described followed by their testing recipe. Microvia reliability test-vehicle fabrication and its thermal cycling are then described. Finally, test vehicle fabrication for via-pad misalignment studies and warpage studies are described.

3.1 Solder-Joint and Dielectric Reliability Test Vehicle (TV)

Test vehicles were fabricated using the sequential build-up process. To compare the reliability performance of C-SiC boards, test vehicles were fabricated both with and without underfill. Conventional dielectric (epoxy) and advanced dielectrics BCB (Benzocyclobutene) and PPE (Polyphenylene Ether) with different film thicknesses were used for fabrication of 200µm pitch test vehicles so as to compare their behavior on C-SiC boards. 100µm pitch 20mm x 20mm flip-chip test-vehicle fabrication is described later. All the test vehicles were built on 12cm x 12cm C-SiC boards.

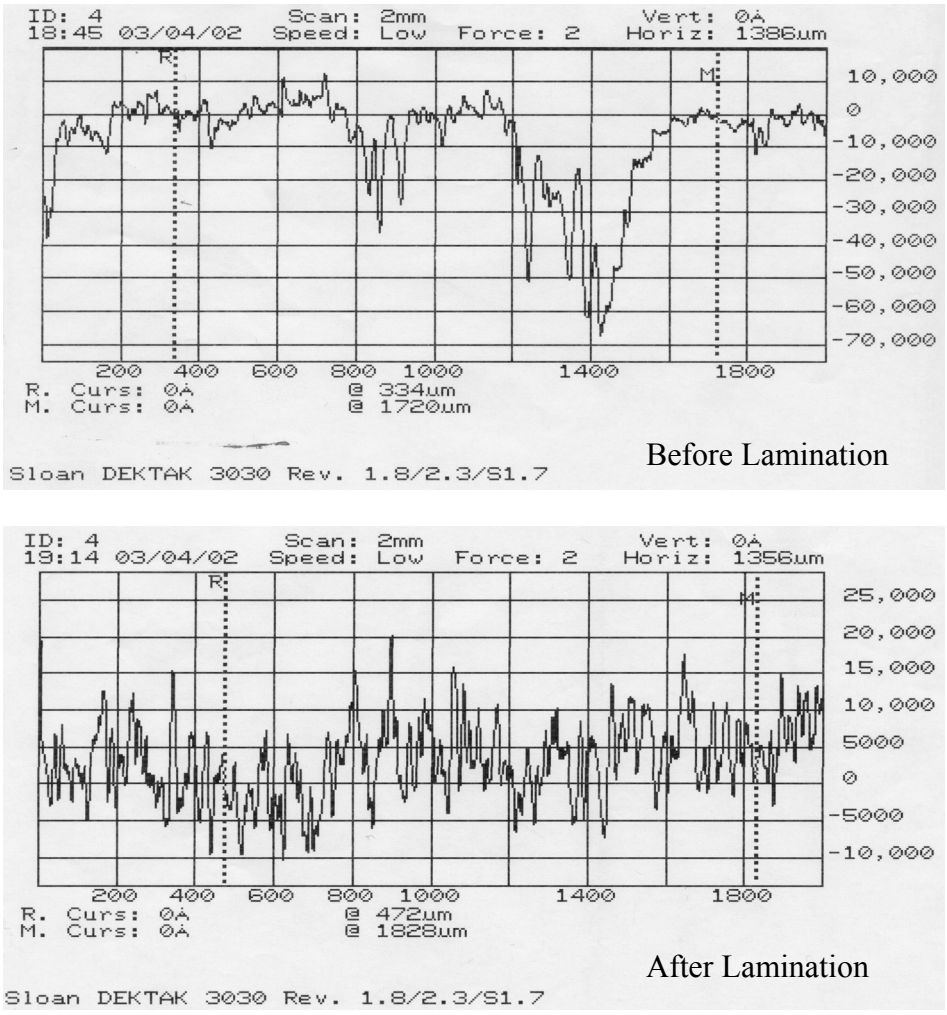


Figure 20: Roughness before and after RCC lamination.

3.1.1 Fabrication of 200µm Pitch TV Using Conventional Dielectric (Epoxy)

The fabrication was done on boards with dimensions varying from 10-12cm, each side. Due to the roughness of the as received boards RCC lamination was done to planarize them. The roughness profile scans before and after lamination as measured using Sloan Dektak 3030® profilometer, shown in Figure 20, depict a significant reduction in roughness from ~6µm to <2µm. Lamination was done using RCC (resin coated copper having 60-70µm thick dielectric layer) from Matsushita's (Koriyama,

Japan) R0880® multilayered PCB materials. Lamination process included two steps, 1) heating at 4.5°C/min for a 20minutes dwell at 90°C and 1 ton load, and 2) heating from 90°C at 2.5°C/min for a dwell of 60 minutes at 175°C and 5.2 ton load for a 5" x 5" board. The copper was patterned and etched to leave the wiring for coupons. The final solder mask coating (25µm) was done with Taiyo® solder mask (PSR 9000 A02® series) composition. Bumped PB-8® dies (Flip-Chip Technology, Practical Components, CA) were assembled on the board with conventional flip-chip process both with and without underfill materials. A commercially available fast-flow, snap-cure underfill (Dexter 4531™, Loctite Corp.) was used. Two boards having 5-6 coupons each were fabricated. Figure 21 shows picture of a fabricated board and the layout of the coupon and daisy chain. Figure 22 shows the process flow sequence used for fabrication of these test vehicles.

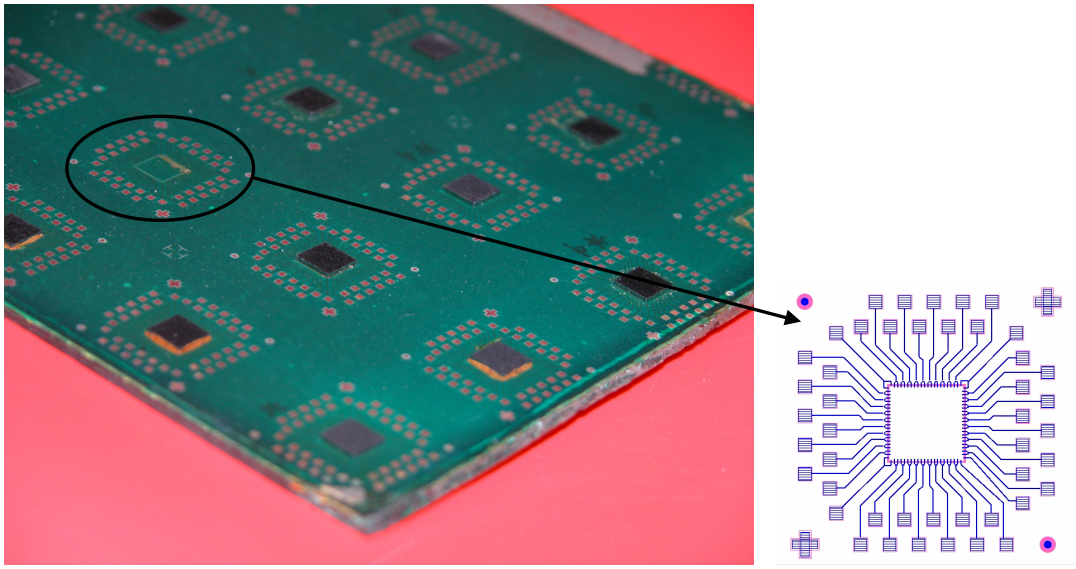


Figure 21: Picture of a flip-chip (200µm pitch; 5mm x 5mm) assembled C-SiC board and coupon daisy-chain layout.

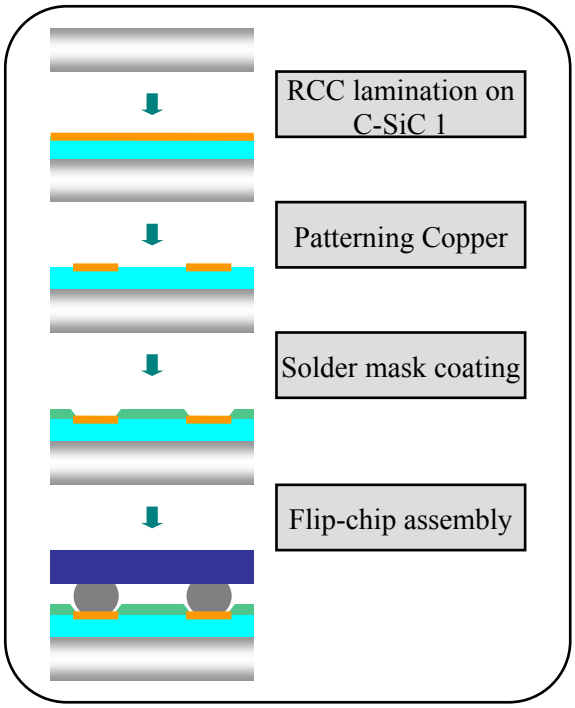


Figure 22: Process flow for test vehicle fabrication with epoxy as dielectric.

3.1.2 Fabrication of 200µm Pitch TV Using Advanced Dielectrics (BCB and PPE)

Two boards having a total of 15 coupons were fabricated for this test vehicle. For enhancing adhesion of BCB (Dow®), AP-3000 (adhesion promoter from Dow®) was spun at 500rpm for 30 seconds and activated thereafter at 90°C for 5 seconds. Cyclotene™ (trade name for BCB, divinylsiloxane bis-benzocyclobutene) grade 3022-46 (40-60% solids content and rest mesitylene) was then spin coated at 1000rpm for 30 seconds. To cure BCB, the temperature was increased to 250°C at the rate of 2°C/min in nitrogen atmosphere followed by one hour dwell at 250°C and cooling to room temperature to yield 5-7µm thick BCB layer. BCB spin coating usually yields a very smooth surface, of the order of 0.5±0.05nm (root mean square value) [46], leading to poor adhesion as

reported by N. Schühler *et al.* [46] in terms of peel force between copper and BCB interface.

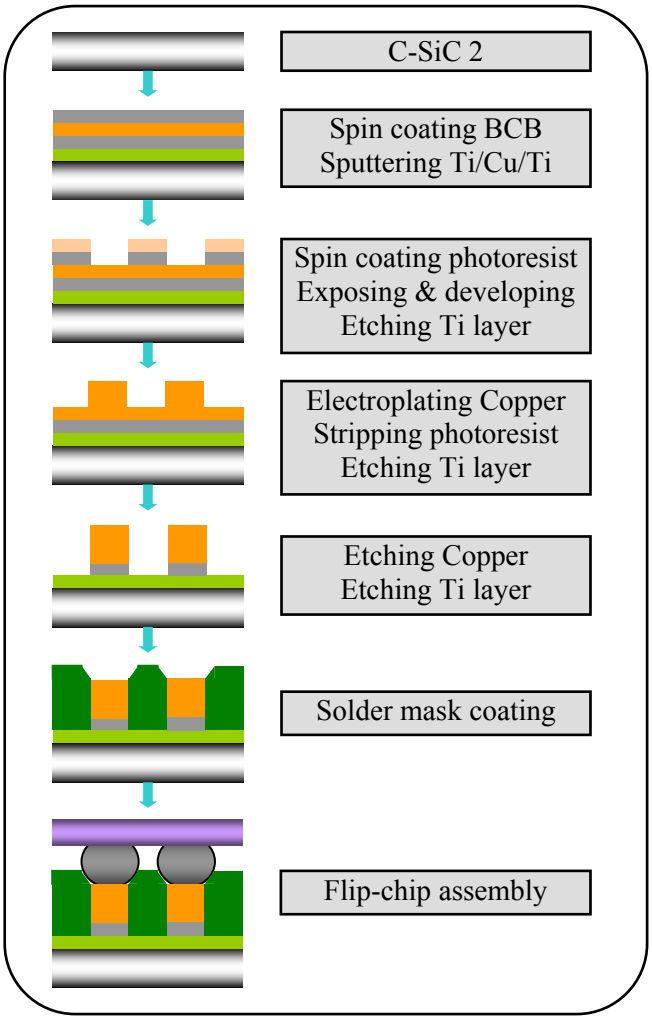


Figure 23: Process flow for test vehicle fabrication with advances dielectrics.

To overcome the delamination and poor adhesion problems, BCB was roughened with a plasma treatment before metallization. This treatment was done at 200mTorr pressure and 200Watts of RF power using 50sccm flow of O_2 and 5sccm of CHF_3 for 4 minutes. To further ensure good adhesion, Ti/Cu/Ti instead Cu was sputtered as the seed

layer. On Ti/Cu/Ti seed layer a negative photoresist Eagle NT-90® was spin coated, exposed and developed. Electroplating is followed by stripping of photoresist, etching off Ti/Cu/Ti seed layer and solder masking (25µm) using the same Taiyo® solder mask (PSR 9000 A02® series). Process flow is represented in Figure 23.

Reliability Test

Test vehicles were subjected to a thermal shock between -55°C to 125°C using liquid media for reliability evaluation. Continuity of the electrical connections was checked every 100 cycles.

3.1.3 Fabrication of 100µm Pitch TV with 20mm x 20mm Flip-Chip Assembly

The fabrication was done by first laminating a polyimide film from DuPont® on the C-SiC boards so as to planarize the surface. At 200°C, 5.5 ton load was applied for 1 hour to laminate polyimide film on a 5" x 5" board. This was followed by sputtering the seed layer of Ti/Cu (15nm/0.5µm). After coating and patterning the resist, copper was electroplated through the resist openings at ~30mA/cm^2 current density for 25 minutes to get 5µm thick copper. The seed layer was then etched off using $H_2SO_4/H_2O_2/H_2O$ (1:1:10) for copper and HF/H_2O (1:10) for Ti. For solder masking, Ciba LM-7081™ (diluted by 10% using PGMEA – Propylene glycol methyl ether acetate) was spin coated at 1600rpm for 30seconds and baked for 14 minutes at 90°C followed by an exposure dose of 1440mJ/cm^2 using UV light of 365nm wavelength. Post exposure bake was done at 110°C for 40 minutes and the solder mask was developed thereafter using gamma-butyrolactone (GBL) for 5 minutes. Final thickness of the solder mask was 4-5µm.

Electroless Ni/Au plating was done (at Peninsula Coating Services, CA) to cover the exposed copper pads. A no clean, no residue flux Fry NR200® from Fry Technologies was sprayed for two seconds. Peripheral area flip-chips (20mm x 20mm) with three rows of Sn0.7Cu solder bumps at 100µm pitch from TLMI® were then assembled with and without underfill to complete the fabrication of the test-vehicle. Daisy-chain design layout for the test-vehicle and the picture of assembled coupon is shown in Figure 24.

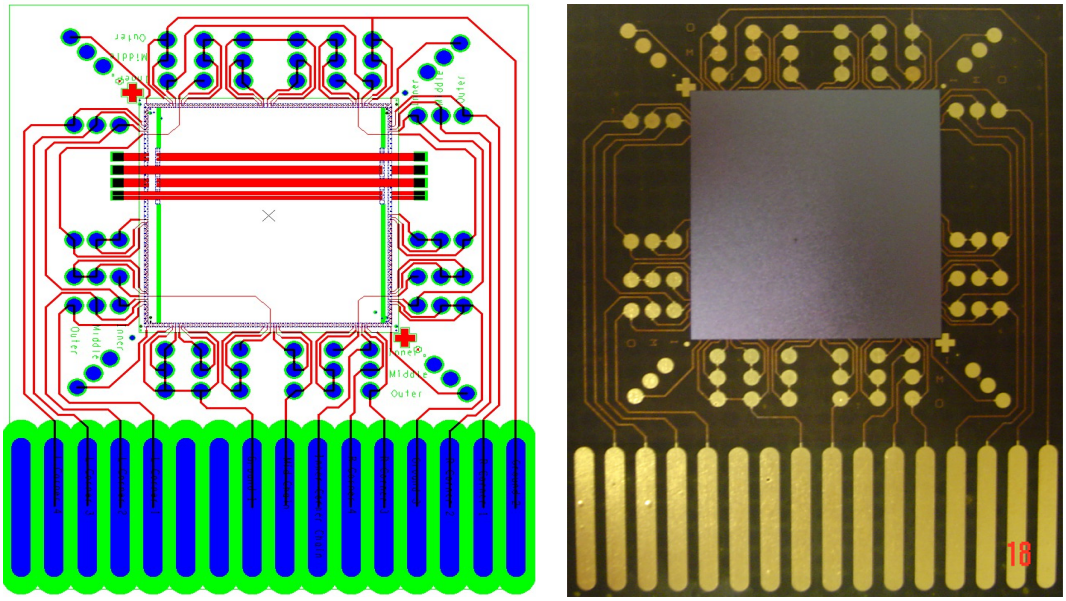


Figure 24: Daisy-chain layout and picture of 100µm pitch flip-chip assembly coupon.

Reliability Test

The reliability was evaluated with air-air thermal shock tests. Test vehicles were subjected to a thermal shock between 0°C to 100°C. The thermomechanical reliability of the electrical interconnections was evaluated after every 100 cycles.

3.2 Microvia Reliability TV

The ITRI-1A test vehicle from the Interconnect Technology Research Institute (ITRI) was used for this study to fabricate metal-via-metal structures. A sequential build-up process with BCB as dielectric was used for fabricating microvia structures. All test coupons consisted of a daisy chain of 8 rows, each having 17 microvias of diameters 50µm, 75µm, 100µm and 125µm. Picture of a coupon is shown in Figure 25. In addition to probing the entire daisy chain, the individual rows can also be probed to isolate the microvia failures.

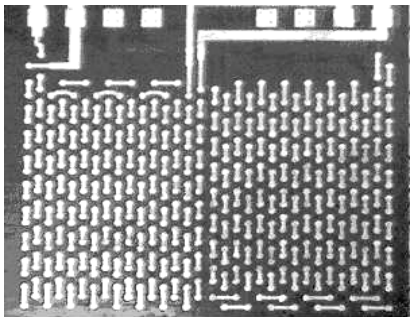


Figure 25: Picture of ITRI-1A test coupon.

Five boards having a total of 22 coupons were fabricated for microvia reliability. The build-up process for fabricating these structures is shown in Figure 26. C-SiC boards were first coated with BCB followed by sputtering of Ti/Cu seed layer. Panel plating was done in order to get 5µm copper which was followed by resist coating, exposing, developing, Cu etching and resist stripping to get the first metal layer with copper pads. BCB was again coated and cured to act as interlayer dielectric followed by sputtering and

patterning of Ti layer as an etch mask. Vitale *et al.* [47] studied the chemistry of BCB etching in $F_2 + O_2$ and $Cl_2 + O_2$ plasmas and suggested that $F_2 + O_2$ plasma is the best in terms of etch rate, anisotropy and low residue. Hence, Reactive Ion Etching (RIE) was done using O_2 and SF_6 gases to form via openings in BCB layer. The RIE conditions included 200mTorr pressure and 300Watts of RF power using 50sccm of O_2, 5sccm of CHF_3 and 0.5sccm of CF_4 to etch BCB at the rate of 0.52µm/min. Ti/Cu was again sputtered as a seed layer for electroplating Cu to 5µm. Finally the top electroplated Cu layer was patterned to complete the formation of microvia test coupons. Optical images of fabricated microvias are shown in Figure 27.

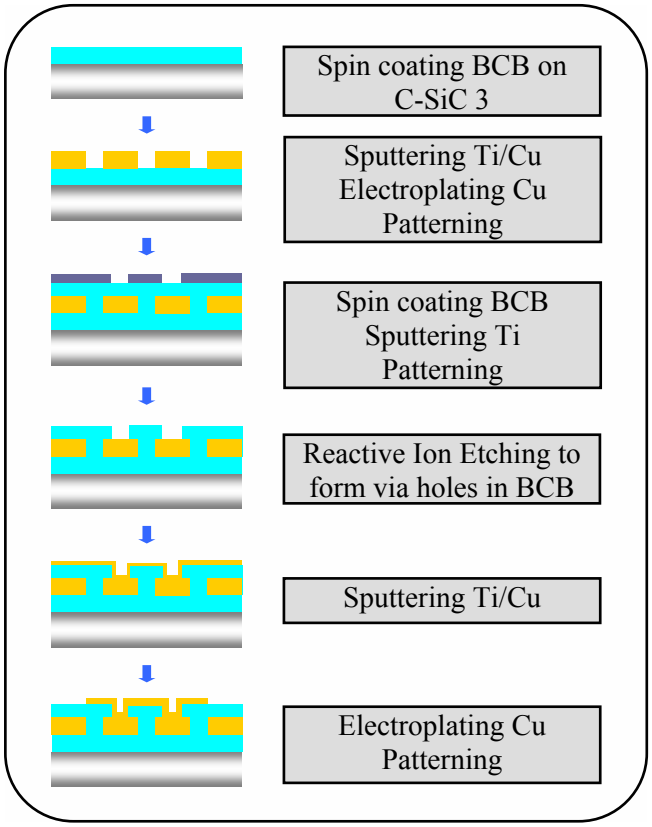


Figure 26: Process flow for fabricating microvia reliability test vehicle.

Reliability Test

Microvia test vehicles were subjected to thermal cycling from -55°C to 125°C in an air-to-air thermal shock chamber. Electrical continuity of the daisy chains was checked every 100 thermal cycles for assessing the reliability.

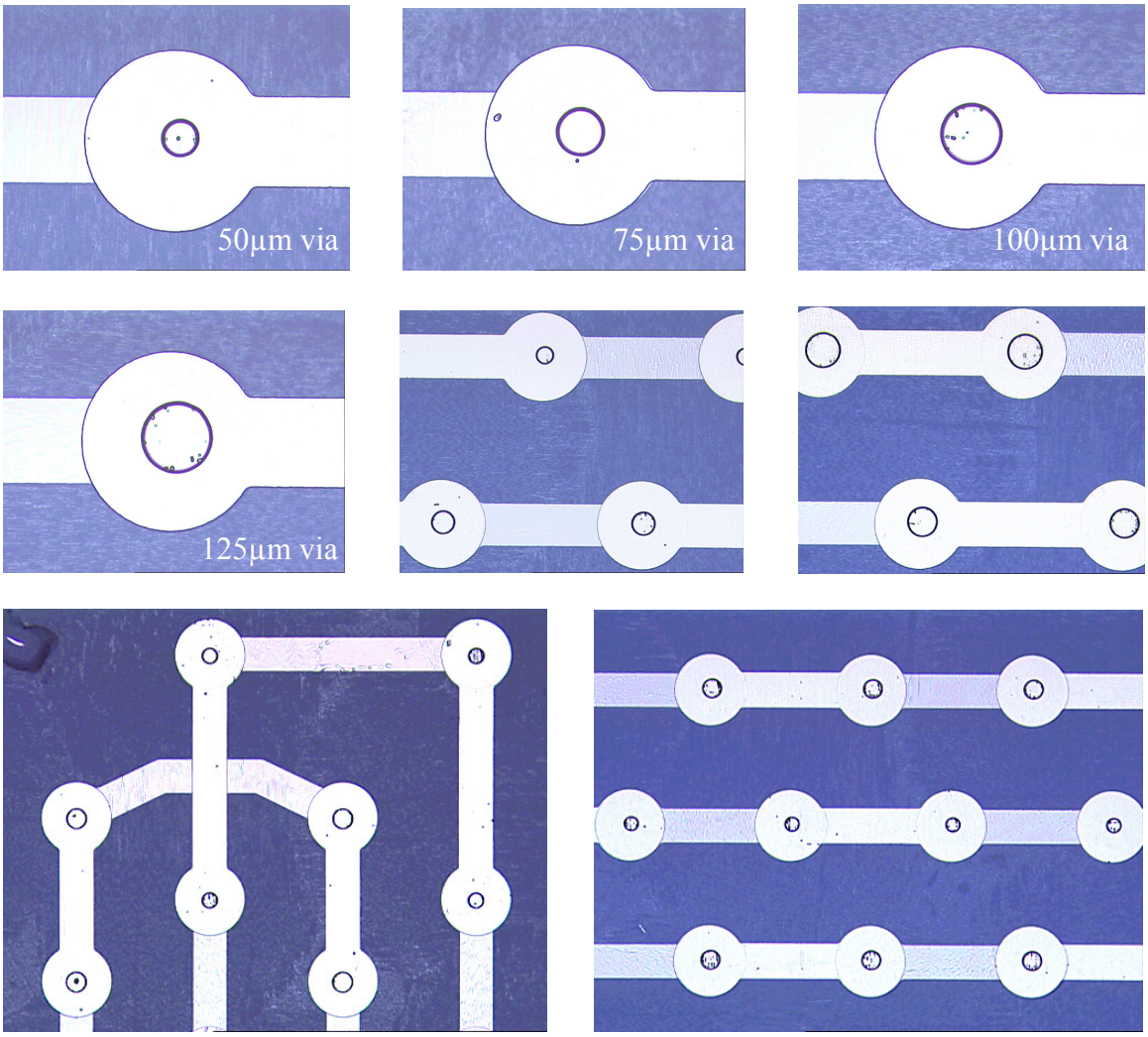


Figure 27: Optical micrographs showing fabricated microvias.

3.3 Via-Pad Misalignment TV

Due to high curing temperature (~250°C) of BCB, test vehicles were fabricated only with C-SiC and not with FR-4. Fabrication included formation of 2µm thick copper pads by sputtering Ti/Cu followed by subtractive etching on a 5" x 5" C-SiC board. Four pairs of copper pads with different distances between their centers were selected for measuring misregistration due to distortion. BCB was then coated to give 8µm thick layer followed by curing which involved heating to curing temperature 250°C at 2°C/min. Dwell time at this temperature was 60 minutes and then the test vehicles were cooled to room temperature at 10°C/min. The distance between the centers of the corresponding pads was again measured and subtracted from the original value so as to get the effective displacement during curing. This procedure was repeated and measurements were taken after coating each layer for a total of four BCB layers.

After curing each BCB layer, the warpage induced was also measured using laser confocal microscopy. For the measurements, the board was kept on a stage which could impart in-pane movement. The out-of-plane tolerance was measured along both the diagonals using a laser confocal microscope. The resulting profile was then fitted with a circle of radius R. The curvature (κ), a reciprocal of radius was calculated after each BCB coating using the warpage values obtained from FEM for both FR-4 and C-SiC.

3.4 Summary

Fabrication steps which essentially included sequential build-up process were described with the help of flowcharts for each of the test-vehicles. The common steps

included were spin-coating, dielectric curing, metal sputtering, photolithography, metal etching, reactive ion etching, electroplating, flip-chip assembly etc. Dimensions and geometry were also described along with details of the processes.

Reliability testing recipes included thermal shock testing of the structures with the exception of via-pad misalignment in which case only the dielectric curing process was considered for testing.

CHAPTER 4

4. RESULTS AND DISCUSSION

This chapter contains both the experimental and FEM results which, in general, are found to be in good agreement. Solder joint reliability results are first discussed for different pitch and solder materials. This is followed by results related to dielectric reliability on low CTE substrates. This chapter then discusses the microvia reliability results. Results of via-pad misalignment studies are then presented and extrapolated to provide results for large panel substrates.

4.1 Thermomechanical Reliability

Thermomechanical reliability of substrates is discussed in terms of solder-joint reliability and dielectric reliability. For evaluating the former, plastic strain accumulated in the stabilized (third) thermal cycle was used as the criterion. Dielectric stresses were calculated as a weighted average of von Mises stresses in the chosen dielectric elements at the end of thermal cycle.

4.1.1 Solder-Joint Reliability and Dielectric Reliability

Figure 28 shows the FEM results obtained as equivalent plastic strain accumulated in stabilized (third) thermal cycle for base substrate boards with different CTEs. 200μm pitch FE model was used with Sn/Pb solder and 30μm epoxy build-up for

these simulations. Table 4 lists the model dimensions used for FEM. It is evident from Figure 28 that plastic strain increases as the CTE of the base substrate deviates from that of Si. In the investigated set of boards, FR-4 showed the highest plastic strain range (~0.13) while a base substrate made up of Si showed the least strain (~2.7E-4). C-SiC boards showed plastic strains (~3.1E-4) very close to that of Si due their Si-matched CTE, indicating that these boards are ideal for having a high solder-joint reliability.

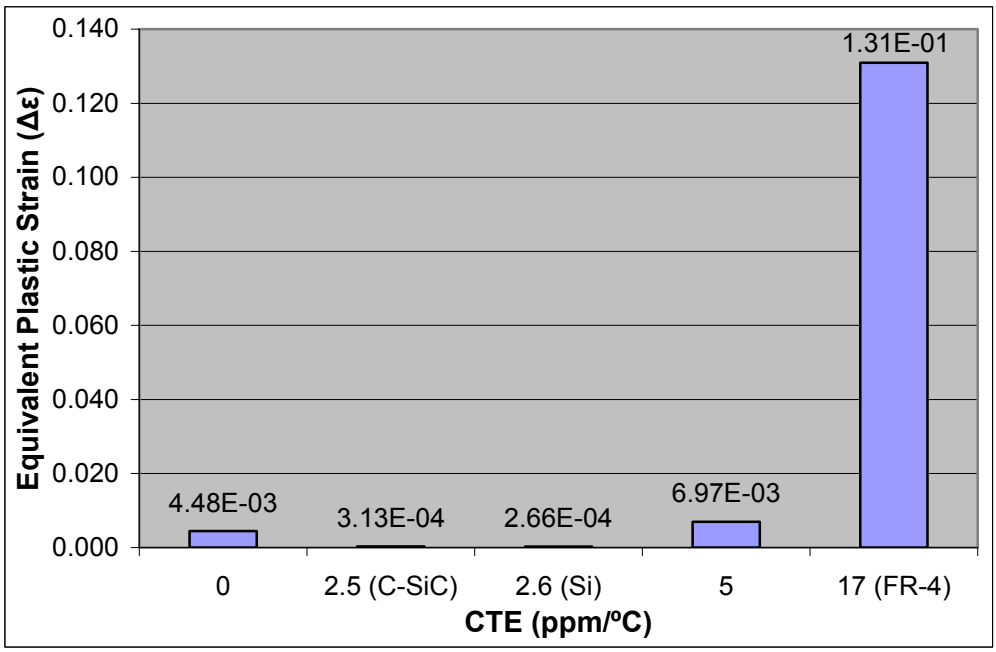


Figure 28: Equivalent plastic strain accumulated in stabilized (third) thermal cycle for base substrates with different CTEs.

For the sake of comparison, fatigue life of the solder-joints was obtained by plugging the plastic strains obtained for different base substrates into Coffin-Manson relation [17] shown as equation 1. Figure 29 compares the fatigue life of flip-chip solder-joints obtained for assemblies without underfill on substrates having different CTEs. Creep properties have not been used for modeling in this work and that is why Figure 29

might be projecting a longer fatigue life. Assemblies on FR-4 showed least fatigue life while C-SiC boards show extremely long fatigue life again emphasizing the high fatigue resistance and hence, high reliability for flip-chip assemblies without underfill.

$$N_f = 0.062(\Delta\varepsilon)^{-2} \qquad \text{..... (1)}$$

where N_f is fatigue life and $\Delta\varepsilon$ is accumulated plastic strain.

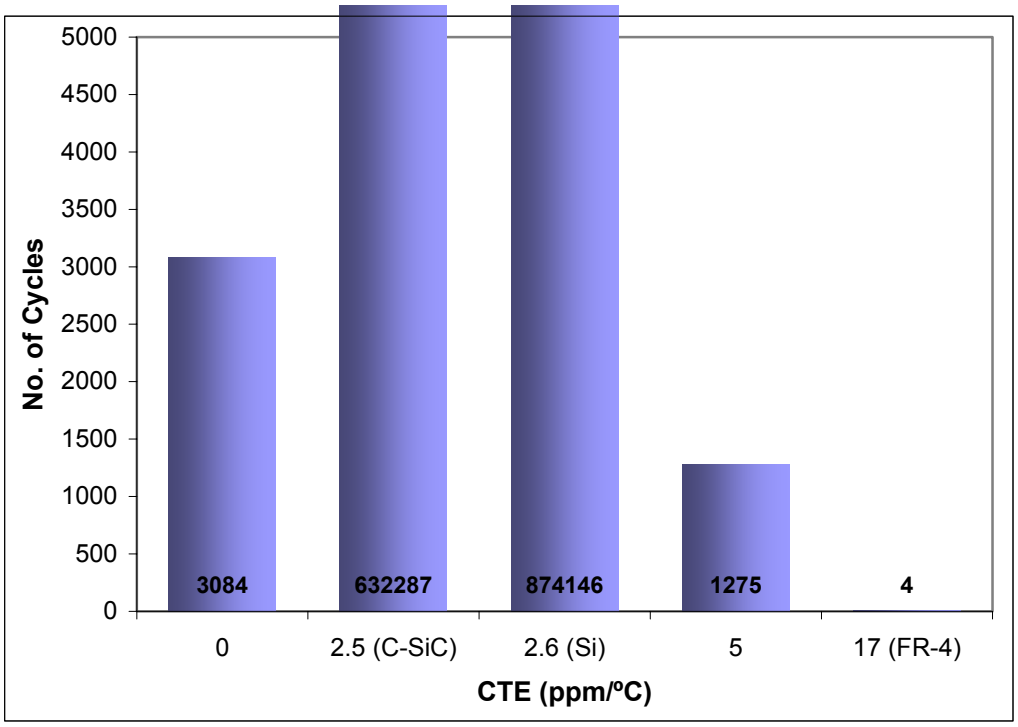
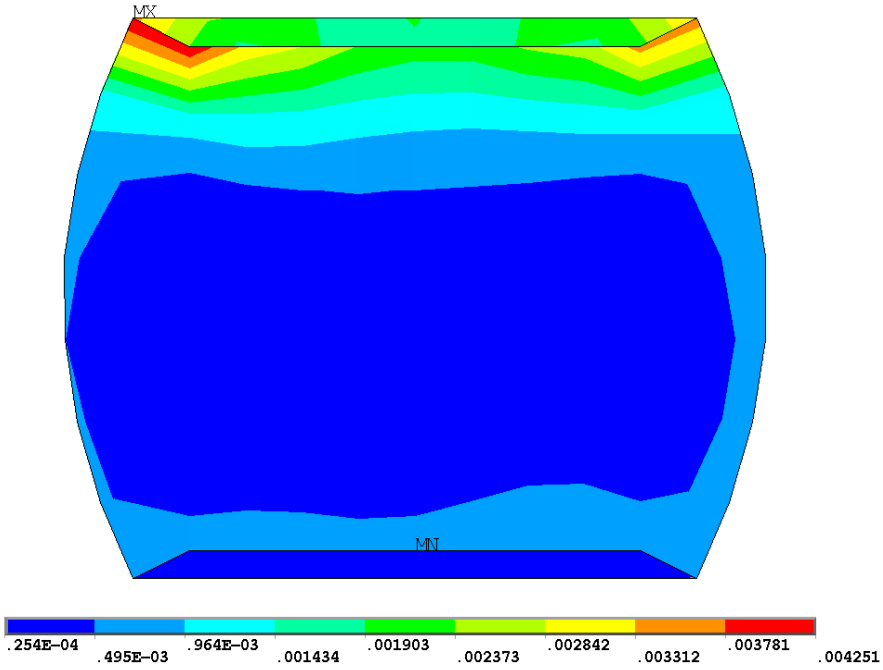
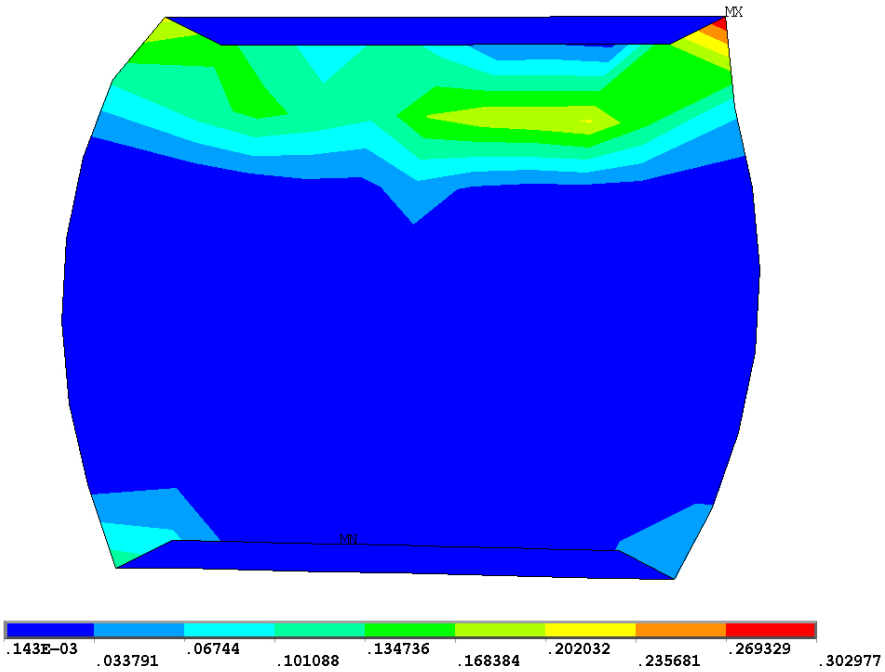


Figure 29: Fatigue life for flip-chip solder-joints on different substrates obtained using Coffin-Manson equation.

Total von Mises strains in solders for assemblies without underfill on C-SiC and FR-4 are shown in Figure 30. In case of C-SiC, the strains (~0.004) are orders of magnitude less than FR-4 (~0.3) indicating high susceptibility of FR-4 and high resistance of C-SiC for solder-joint failure.



(a)



(b)

Figure 30: Total von Mises strains in the solders (a) for C-SiC, and (b) for FR-4.

Stress analysis in the dielectrics was done with FE modeling to understand the dielectric behavior in different test vehicles. To evaluate their influence on dielectric stresses, different dielectrics with different thicknesses were modeled. Figure 31 shows the total von Mises stress in the selected (Section 2.2) elements of the dielectric and the average dielectric stress value.

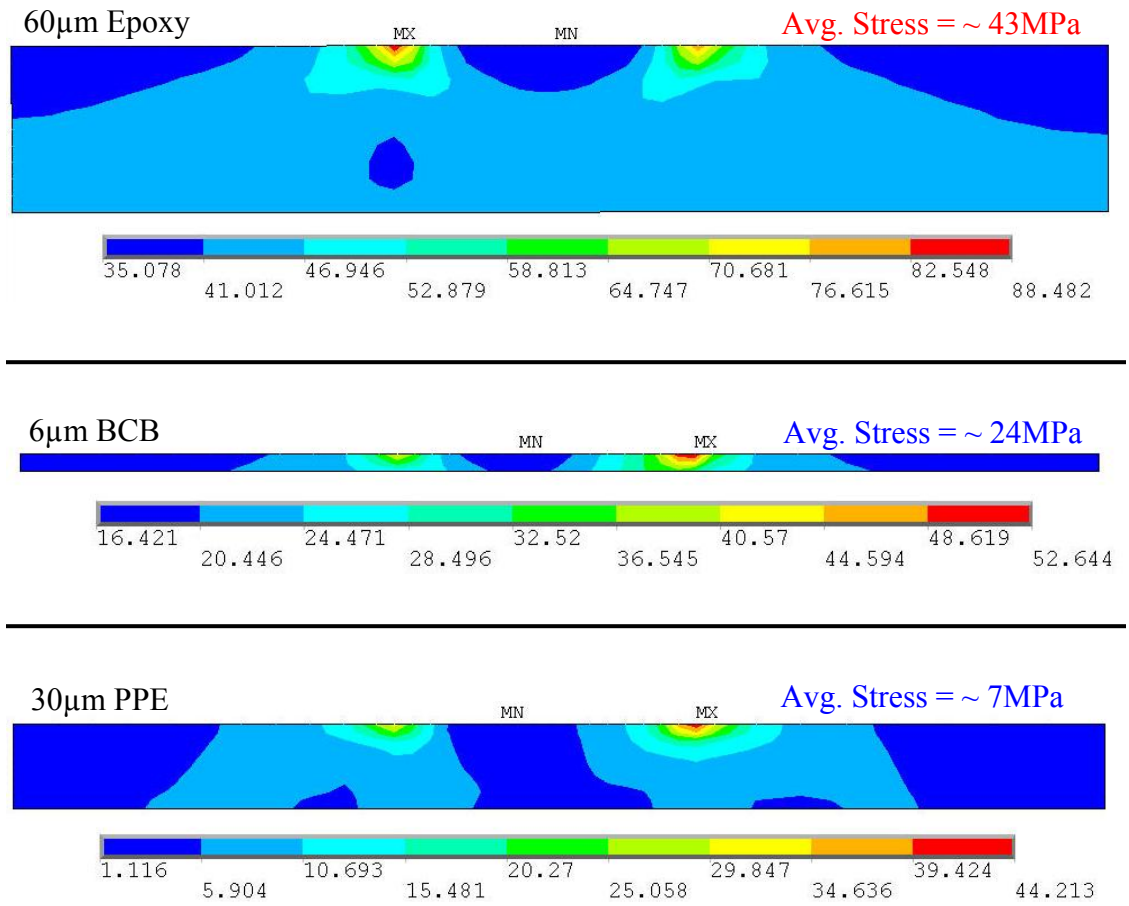


Figure 31: von Mises stress in different dielectrics as obtained from FE simulations.

It can be seen from Figure 31 that the dielectric stresses for 60µm epoxy build-up are quite high ranging from ~82-88MPa in the stress concentrated areas with an average of ~43MPa over the whole dielectric. These stresses are ~48-52MPa with an average of ~24MPa for 6µm BCB build-up. For a 30µm build-up with PPE which is a very low CTE (13ppm/°C) dielectric, the dielectric stresses as shown in Figure 31 are minimum, averaging ~7MPa. Therefore, it can be inferred that the dielectric thickness and its CTE are the major factors contributing for the dielectric stresses. This has been reported earlier for a different set of materials by Hegde et al [48].

Table 10: Experimental results for thermal shock tests

Substrate (CTE ppm/°C, Modulus GPa)	Dielectric (CTE ppm/°C, Modulus GPa)	Thickness for build-up (µm)	Cycles to failure	Primary failure mode
FR-4 [14] (17, 20)	Epoxy (60, 3.5)	60-70	<100	Solder-joint cracking
C-SiC 1 (2, 80)	Epoxy (60, 3.5)	60-70	300	Dielectric cracking; Copper line cracking
C-SiC 2 (2, 150)			500	
C-SiC 2 (2, 150)	BCB (45, 2.5)	5-10	**>1000**	Minimal dielectric cracking
C-SiC 2 (2, 150)	PPE (15, 2.4)	30	**>1000**	Minimal dielectric cracking

Experimental results of thermal shock tests are listed in Table 10. Results for FR-4 are taken from an earlier work [14].Table 10 shows that the test-vehicles fabricated

with FR-4 and without underfill, as studied by S. Bansal [14] for similar die and fabrication conditions, failed within the first 100 cycles of thermal shock testing which is predicted by FE models as shown in Figure 29.

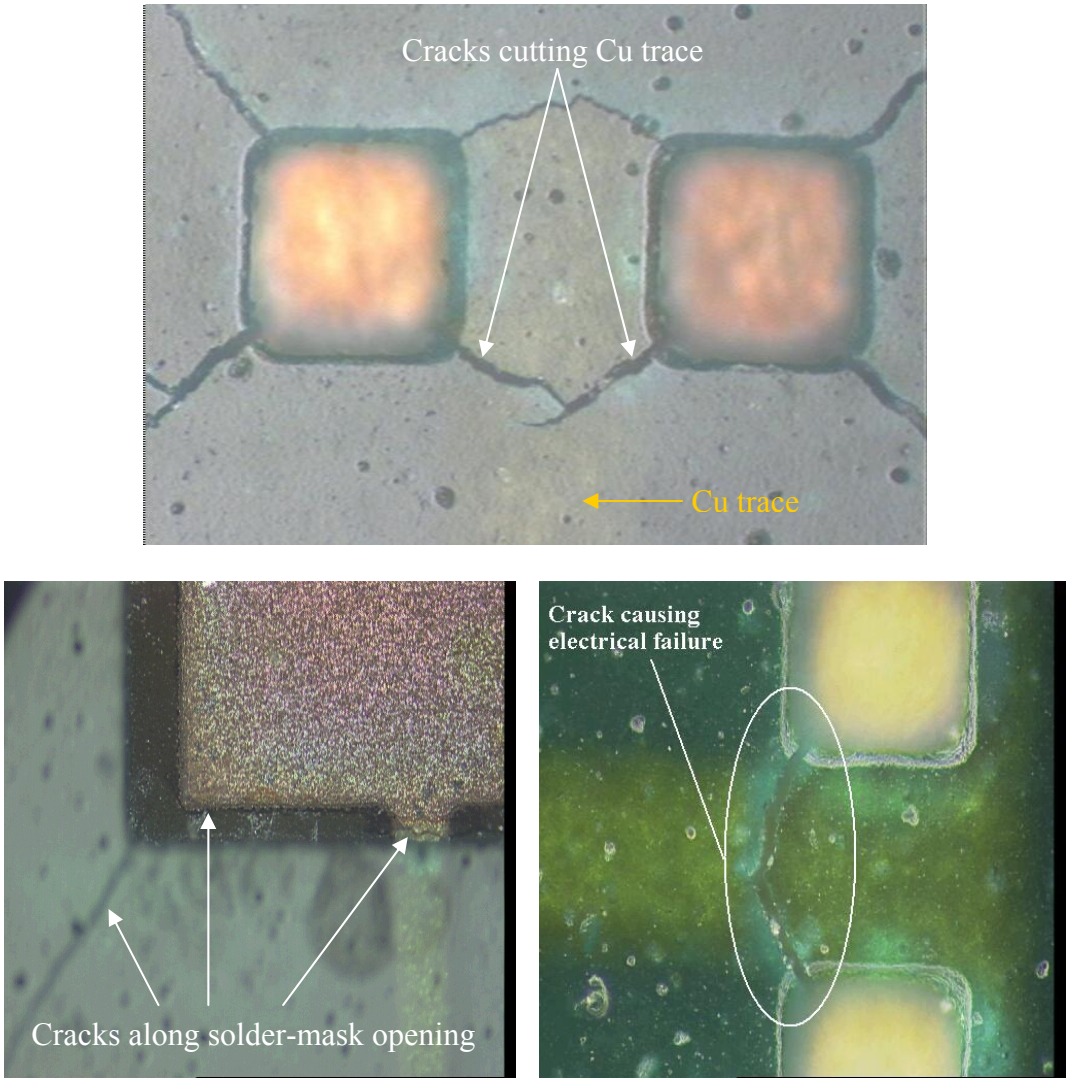


Figure 32: Dielectric cracking as failure mode for test vehicles with thick (60-70µm) epoxy dielectric on C-SiC (low CTE) boards.

With thicker dielectric build-up: The low stiffness composite board (C-SiC 1) did not show any failure in the solder joints even after 500 cycles because of its close CTE with that of Si. The flip chip daisy chain was completely connected though some of the pads showed high resistance implying that the failure was within the lines and not in the solder joint connected through the daisy chain. However, severe dielectric cracking, as shown in Figure 32 was observed at the corners of the square solder mask openings near the testing pads and the daisy chain, and along the edges of the solder mask openings. These cracks originate from the stress concentration at the corners of the square openings and also seen to penetrate through the copper lines. Cracks within the copper lines, independent of dielectric cracking were also observed within the solder mask openings when the stiffness of board is low (<80GPa). Boards with moderate stiffness ~150-170GPa (C-SiC 2) also showed significant dielectric cracking.

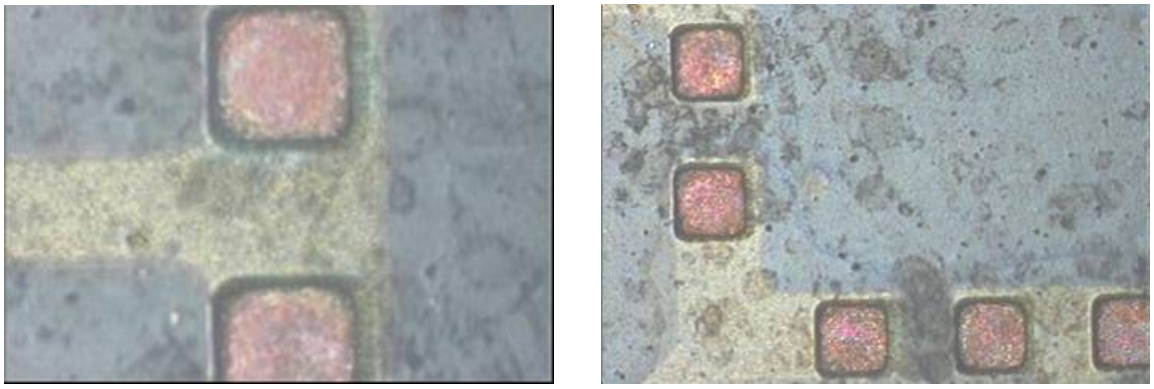


Figure 33: No dielectric cracking in 30µm PPE and 6µm BCB build-up test vehicles.

With thinner dielectric build-up: With C-SiC 2 boards, negligible dielectric cracking was observed in the test vehicles with thinner BCB or PPE build-up as compared to thicker

epoxy build-up. The test vehicles with both these dielectrics build-up showed no dielectric cracking over 1000 cycles as shown in Figure 33.

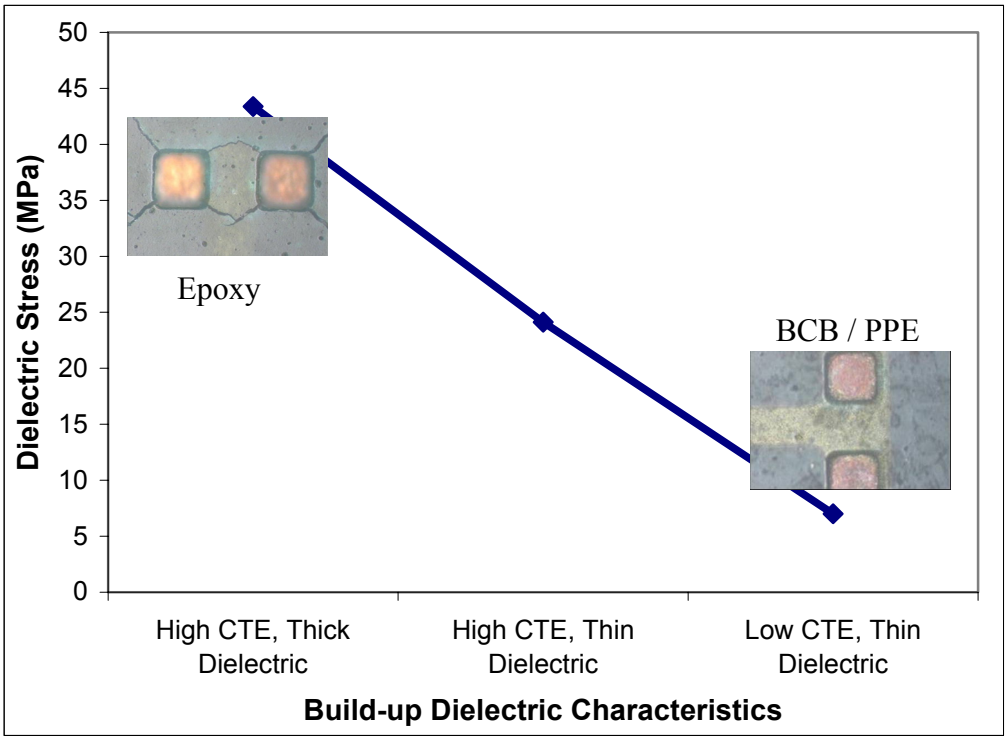


Figure 34: Averaged von Mises dielectric stress as modeled in single-layered test vehicles for low CTE boards.

Figure 34 shows dielectric stress variation with dielectric characteristics. It can also be seen from Figure 31 and Figure 32 that the stress concentration areas lie at the ends of the pad openings mostly at the corners leading to the observed dielectric cracking at the pad corners. Both FEM results and experimental observations conform that this is more predominant when high CTE thick dielectric was used for the build-up as shown in Figure 34.

To illustrate the effect of solder pitch and die size on thermomechanical reliability of flip-chip assemblies on C-SiC, von Mises strains after cooling from reflow temperature (~183°C for Sn/Pb) to room temperature are plotted as shown in Figure 35. Total von Mises strain, as shown in Figure 35, increases exponentially with reduction in pitch of solder balls in agreement with the results obtained by S.Bansal [14]. This exponential increase in strains with reduction in pitch is even more severe as the die size is increased from 5mm x 5mm to 20mm x 20mm, emphasizing lower thermomechanical reliability of fine-pitch large die packages.

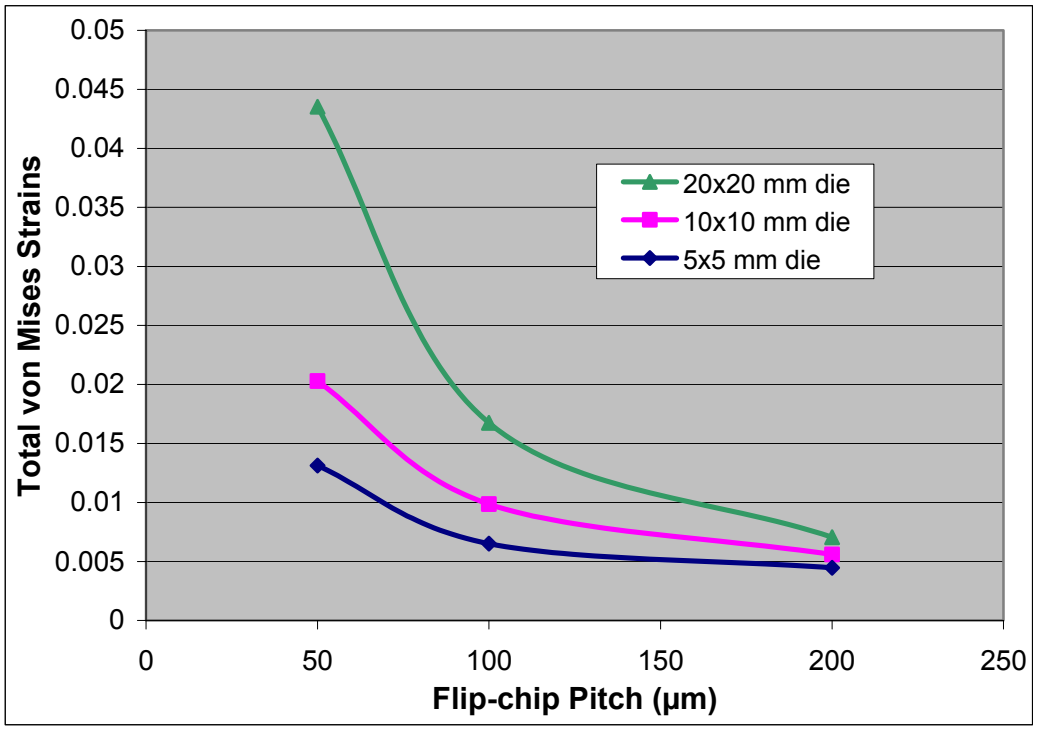


Figure 35: Total von Mises strains after cooling from reflow temperature (~183°C) to room temperature illustrating the effect of die size and solder pitch.

(FE model details: 60µm epoxy build-up, 2.2ppm/°C substrate and one peripheral row of solder)

Thermomechanical reliability of solder-joints has a large dependence on the solder material. To evaluate and compare the reliability of lead-free solder on C-SiC without underfill, modeling with SnAg solder was done. Figure 36 shows the accumulated plastic strain and corresponding fatigue life obtained using Coffin-Manson relation (equation 1) for C-SiC. The accumulated strain is higher in SnAg solders than conventional SnPb solders as was observed in terms of fatigue life by Schubert *et al.* [49]. Even with higher strain in SnAg solders, the fatigue life prediction using equation 1 gives ~19000 cycles to failure. These results predict that C-SiC shows very good thermomechanical reliability even with SnAg solders.

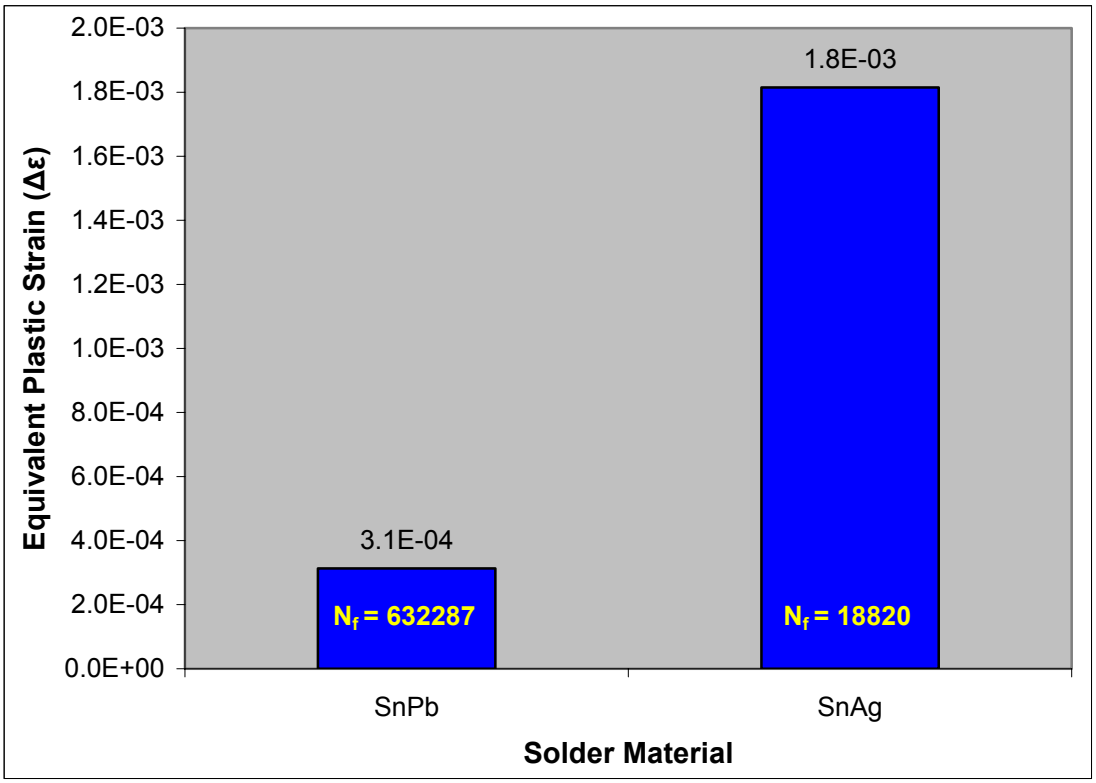


Figure 36: Equivalent plastic strain accumulated in stabilized (third) thermal cycle for different solder materials on C-SiC. (Model parameters are given in Table 2)

To evaluate the reliability performance of large-die flip-chip assemblies with 100µm solder pitch on C-SiC, FE models were developed along with experimental analysis. As mentioned earlier, the test vehicle has 3 peripheral rows of solders. Simulations predicted that, although there is not much difference in the von Mises strain (Figure 37) value for the each row of solders yet the innermost (smallest distance from the neutral axis) row of solders has the highest strain. This is contradictory to the common belief which assumes that greater the distance from the neutral axis, more is the strain. This result may not be true in all cases depending upon the number of rows of solders, solder-pitch and die-size, and a more in-depth analysis, which is beyond the scope of this work, is needed to correlate all these parameters to predict this behavior.

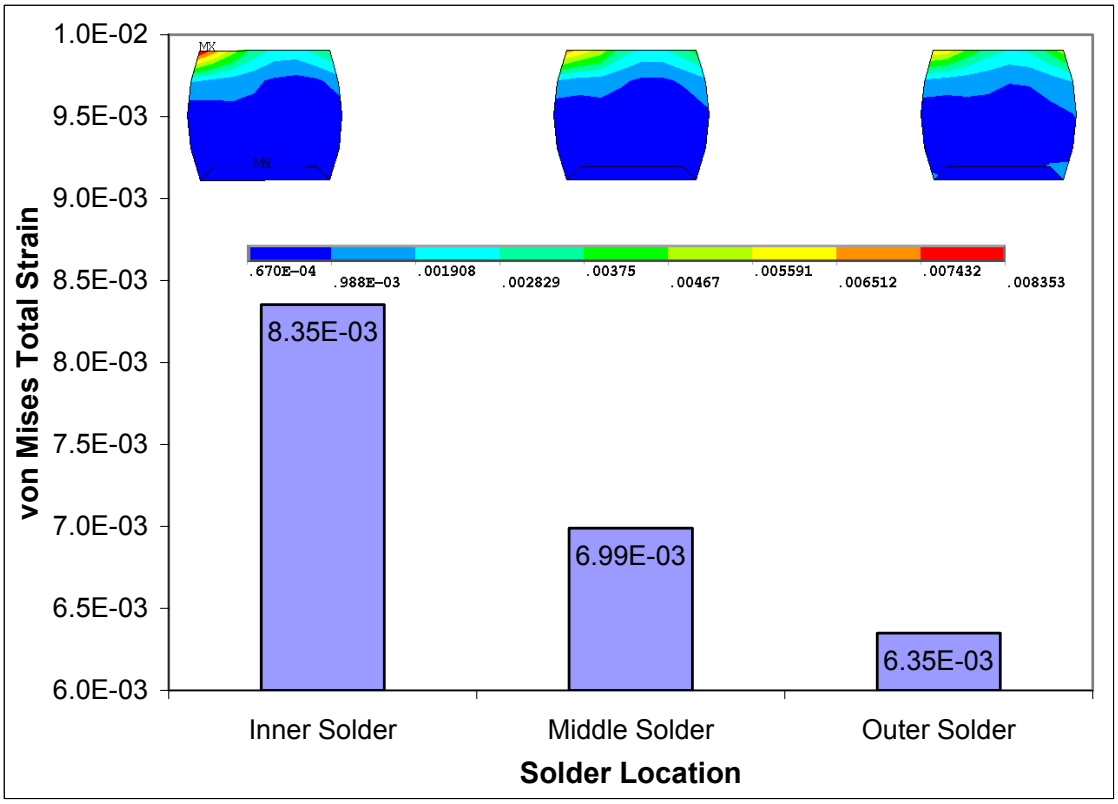


Figure 37: von Mises strain in the solders.

Similar trends can be observed in the accumulated plastic strain values of the solders. Figure 38 shows the plastic strain accumulation history for the innermost solder that shows the highest accumulated plastic strain ~5.3E-4 which translates to a fatigue life of ~220000 cycles when plugged in to equation 1. This low plastic strain and, in turn, high fatigue life indicate very good reliability even for a very large die (20mm x 20mm) having fine solder pitch (100µm). High reliability for such a large die at fine pitch is a result of having three peripheral rows of solders instead of one in which case the accumulated plastic strain is ~1E-3 (fatigue life ~65000). The CTE mismatch being taken up by three rows of solders having approximately three times the number of solder bumps than in a one peripheral row of solders accounts for the lower strain in the former case.

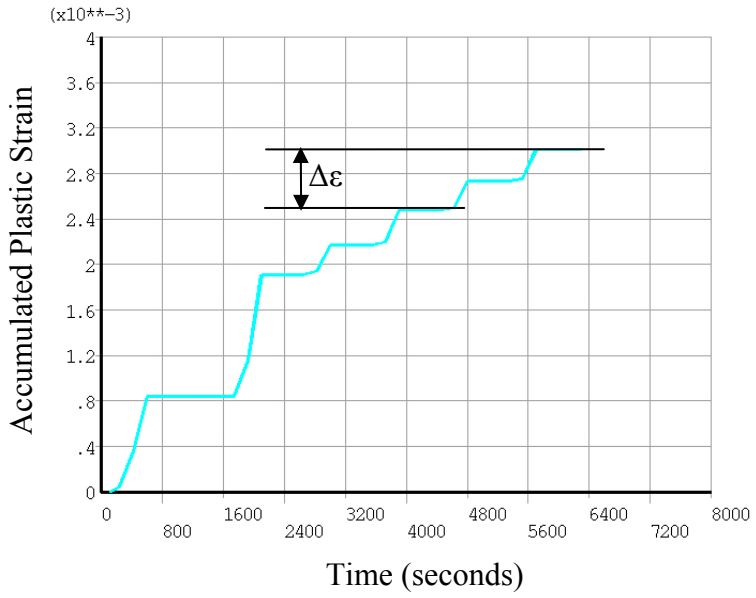


Figure 38: Plastic strain accumulation history for the innermost solder row.

Test vehicle with 20mm x 20mm flip-chip having 100µm pitch lead-free (Sn0.7Cu) solders assembled without underfill was subjected to thermal shock test in air from 0°C to 100°C. The test vehicles survived more than 1000 cycles without any significant increase in resistance. The increase in resistance at the completion of 1000 thermal cycles was less than 3% of the original resistance at 0 cycles for all the daisy chains in all test vehicles. No failure was observed in any daisy-chain. Optical image analysis showed no dielectric cracking. The results are tabulated in Table 11.

Table 11: Thermal shock test results for 100µm pitch TV

Substrate (CTE ppm/°C, Modulus GPa)	Dielectric (CTE ppm/°C, Modulus GPa)	Thickness for build-up (µm)	Cycles to failure	Primary failure mode
C-SiC 2 (2, 150)	PI (17, 2.5)	30	**>1000**	No failures

4.2 High Wiring Density

High density wiring capability of C-SiC is evaluated and discussed with respect to two aspects – microvia reliability while thermal cycling and via-pad misregistration during processing. Both FEM and experimental results are discussed in the following sections. In some cases, simulations results for different boards and dielectric materials are compared to predict the suitability of the boards for multilayer high-density wiring.

4.2.1 Microvia Reliability

Equivalent plastic strains after three thermal cycles for different via diameters, shown in Figure 39, suggest that as the via diameter increases, the plastic strains decrease and hence the via reliability increases [50]. These results are in accordance with the results reported in previous works [51], wherein, on the basis of numerical modeling, the authors have also showed that the smallest microvia survives least number of thermal cycles. The increasing trend of via strains with decreasing via diameter (Figure 39) also leads to the direct inference that moving towards smaller via diameters (~10μm) may result in excessively high via strains. Micro-scale plasticity effects, not considered in this work, are estimated to compensate with some of the increase in via strains (Figure 39) as described by Ramakrishna et al. [52]

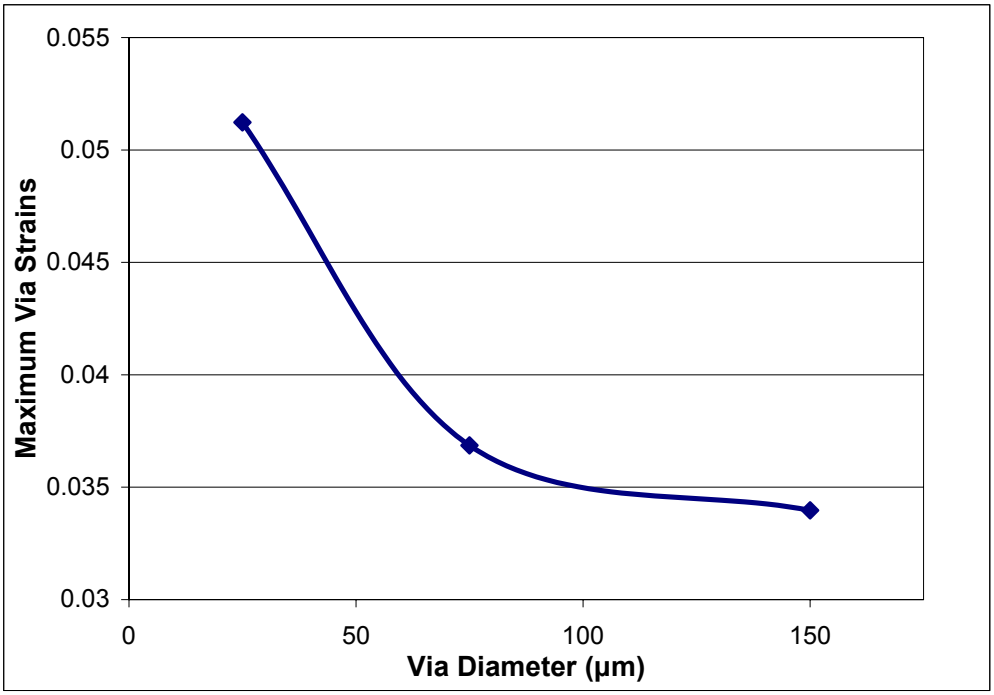


Figure 39: Plastic strain simulation results for C-SiC/BCB test vehicle with different via diameters.

The Cu-BCB microvia structures when subjected to air-to-air thermal shock tests from -55°C to 125°C survived 1200 cycles (Table 12) without any failures. Modeling results indicate that the lower the via diameter, higher are the strains. The experimental results correspondingly show highest increase in resistance after thermal cycling with the smallest via diameters (50μm).

Table 12: Microvia reliability test results

Substrate (CTE ppm/°C, Modulus GPa)	Dielectric (CTE ppm/°C, Modulus GPa)	Thickness (μm)		Cycles to failure
		Metal (1& 2)	Dielectric	
C-SiC 3 (2, 180)	BCB (45, 2.5)	5	5	**>1200**

Results of simulations [50] for same diameter (25μm) and different dielectric layers signify that the via strain after thermal cycling is the least in case of PI and highest in case of epoxy with BCB in between these two as shown in Figure 40. The value of strain for Case 2 (C-SiC 3/Epoxy) is 7.5% (Figure 40) which is higher than the experimentally measured [53] yield-strain value of acid-plated copper which is 7.4%, indicating that the copper in this case is in the plastic region and has a higher probability of failure during fatigue testing. It is also evident from Figure 40 that with everything else remaining the same, higher the CTE of the dielectric, more are the strains induced in the copper after thermal cycling which agrees very well with the results reported in past [53].

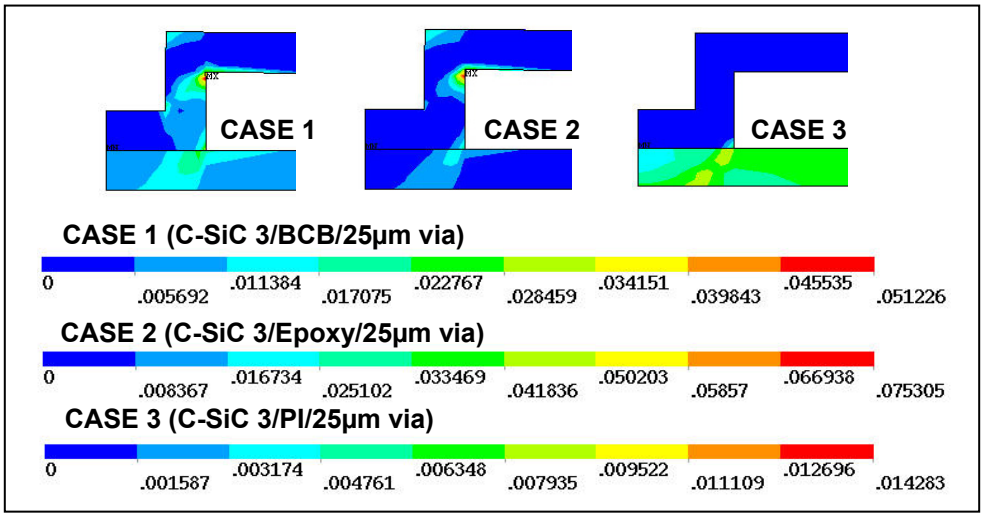


Figure 40: Via strains after thermal cycling with different interlayer dielectrics. The via diameter is 25 µm.

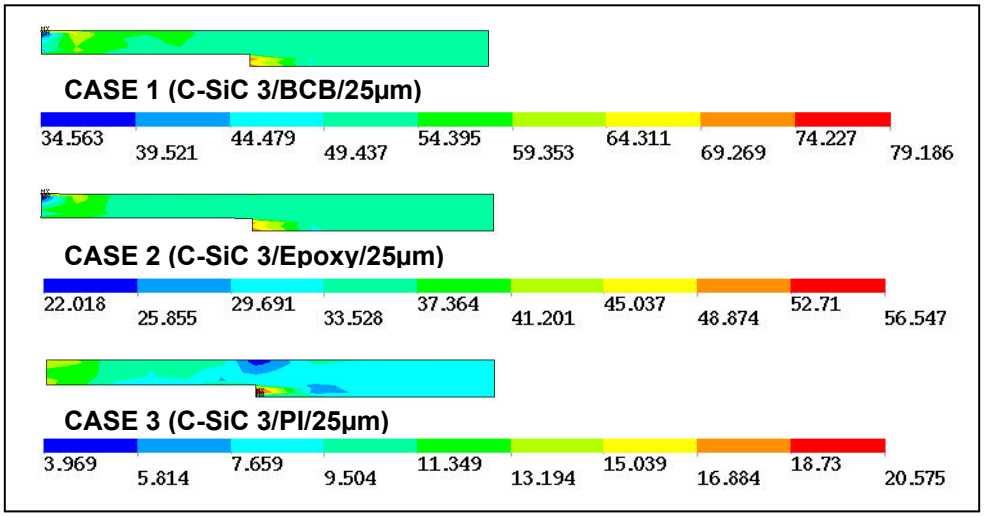


Figure 41: Dielectric stresses after thermal cycling.

Figure 41 shows the dielectric stresses for different build-ups after thermal cycling. C-SiC/PI shows the lowest dielectric stresses. C-SiC/BCB shows higher stresses

than C-SiC/Epoxy because the curing temperature of BCB (~250°C) is much higher than the curing temperature of epoxy (~135°C). Cooling from curing temperature to room temperature therefore induces higher stresses in BCB than epoxy, but even with higher stresses no delamination or cracking of BCB was observed.

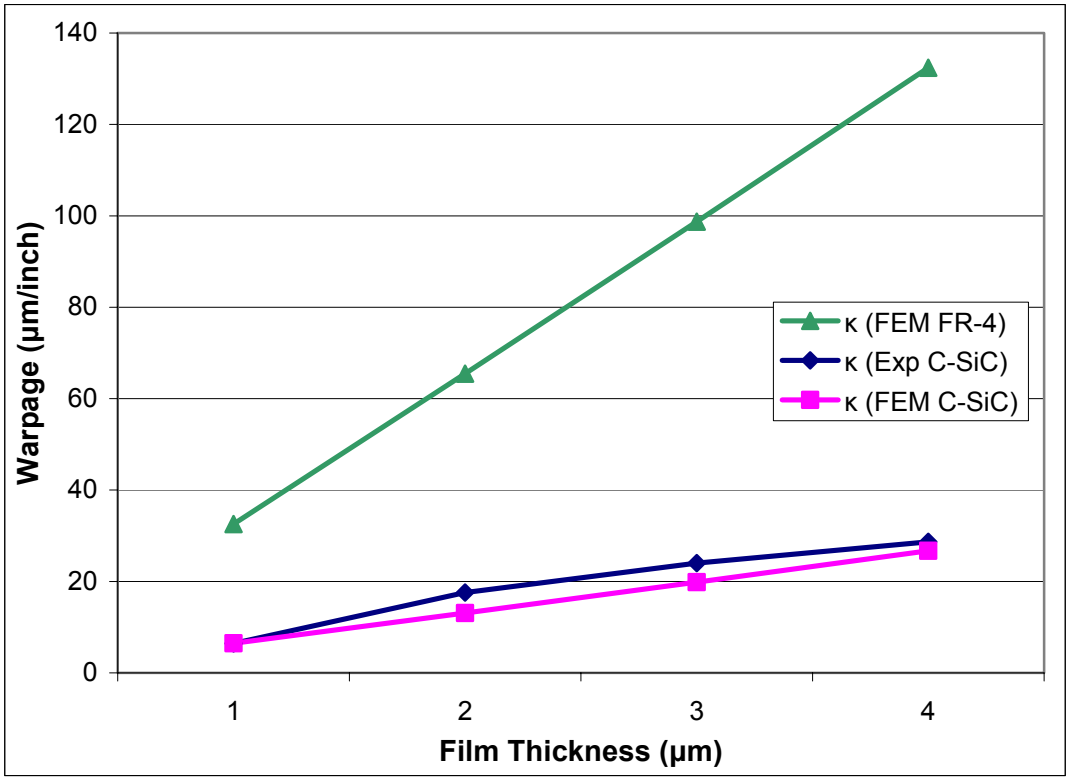


Figure 42: Warpage values after curing different BCB layers (calculated at 1 inch from the board center along the diagonal).

4.2.2 Warpage and Via-Pad Misalignment

The curvature κ was calculated after each BCB coating using the warpage values obtained from FEM for both FR-4 and C-SiC. These values, used to calculate warpage, are shown along with experimental results in Figure 42 and lie within the same range as

obtained earlier for a different set of materials by Banerji et al. [8]. It is evident from Figure 42 that the results from FEM conform well to the experimental results for C-SiC, thus validating the FE model. Moreover, Figure 42 reveals that the warpage values for the same number of BCB layers is ~5-6 times higher for FR-4 than for C-SiC. Smaller curvature and warpage of C-SiC indicates that it is more resistant to warping because of its higher modulus, thus making it much less susceptible to via-pad misregistration.

The via-pad misalignment induced due to coating of one BCB layer (8µm) is shown in Figure 43. The more the distance between the vias, more is the misregistration as depicted in Figure 43. In addition, misalignment in case of FR-4 is about 5 times more than C-SiC, making C-SiC a much better option for multilayer structures to achieve high wiring density.

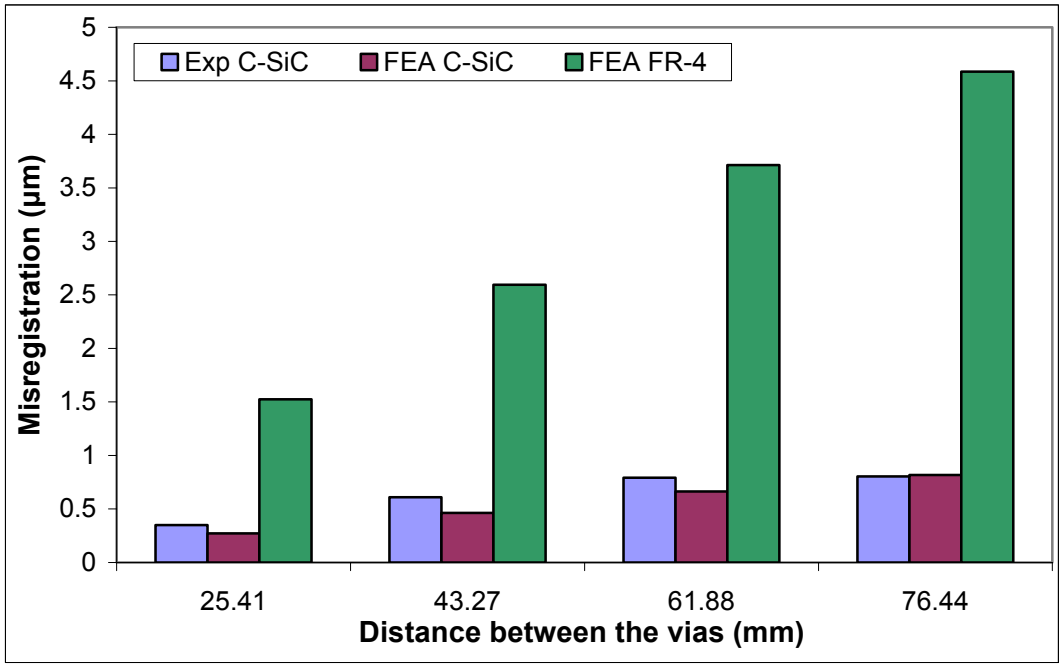


Figure 43: Via-pad misalignment by curing one layer (8µm) of BCB.

Via-pad misregistration after curing each layer of BCB is shown and compared with the FEA results in Figure 44. For a distance of ~76mm between the vias, the misregistration after fabricating 4 layers (8µm each) of BCB is ~6µm/inch for FR-4 as opposed to a much lower value of ~1µm/inch for C-SiC.

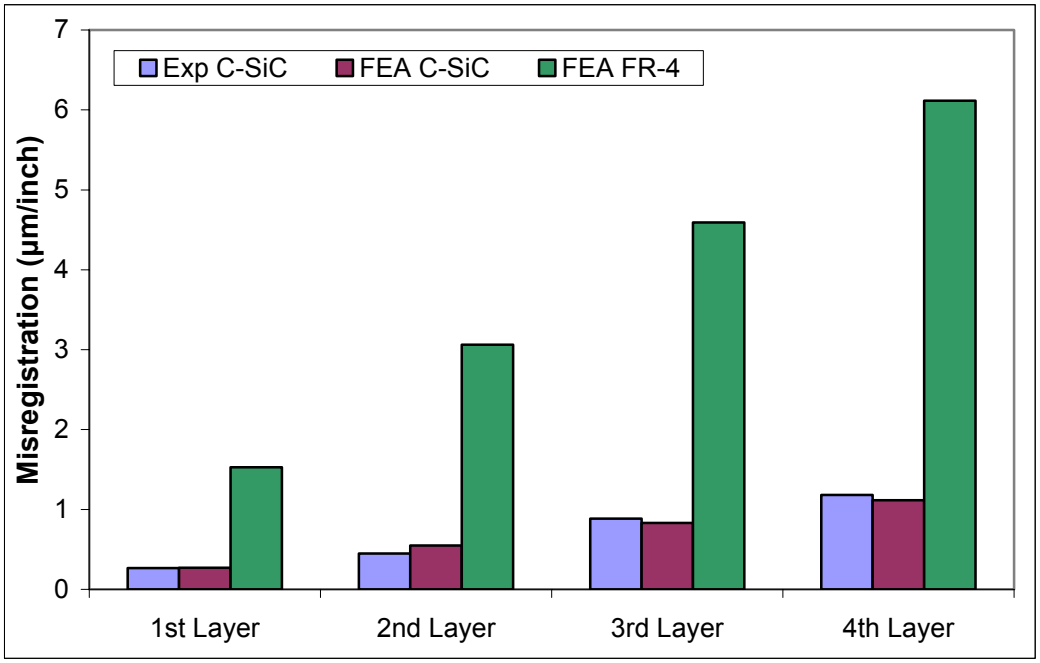


Figure 44: Misalignment after curing different layers (8µm each) of BCB for via distance ~76.44mm (calculated at 1 inch from the board center along the diagonal).

Similar approach was adopted to extend the FE model and approximate the misregistration for a 300mm x 300mm board (~400mm distance between the vias situated diagonally opposite) with 4 layers of 8µm thick BCB. As shown in Figure 45, the misregistration obtained after extrapolation is ~17µm for C-SiC (180GPa) and ~96µm for FR-4 (24GPa), which clearly indicates that FR-4 would not be suitable for needs of forming 25µm vias with 50µm capture pads in such a configuration. However, C-SiC can

cater to such stringent requirements for high density wiring due to much lower via-pad misregistration. The goal is to have C-SiC boards of modulus ~350GPa which, as shown in Figure 45, will have an extremely low misregistration of 7.52µm across 400mm distance enabling formation of 20µm vias on 30µm capture pads.

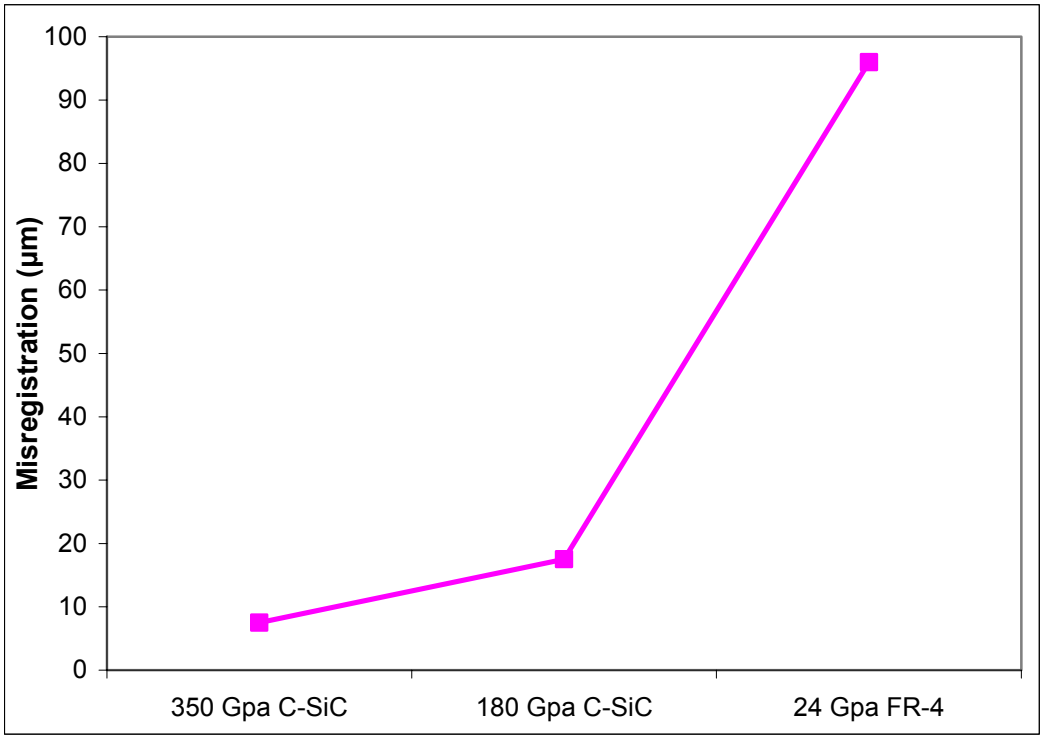


Figure 45: Extrapolated via-pad misalignment values for different boards having 4 BCB layers (8µm each) and via-distance ~400mm.

4.3 Summary

The high stiffness C-SiC boards with thinner BCB dielectrics did not show failures related to dielectric cracking or solder joint fatigue. Experimental results matched well in case of dielectric stress analysis. As predicted by FE modeling no failures while

thermal shock testing were observed even for large die having solders at fine pitch. While finer via diameters could aggravate the microvia strains, a combination of low CTE and high-strength dielectrics can address the reliability problem in multilayered structures. Microvia reliability was shown for two metal layered structures on C-SiC. FEM and experimental results for via-pad misregistration indicate the superiority of C-SiC over FR-4 and its suitability for high-density multilayer structures with small padless vias.

CHAPTER 5

5. SUMMARY AND FUTURE WORK

This chapter is divided into two sections. First section summarizes the work done and contains conclusions that can be drawn from it. Second section explores the scope of future work so as to further this work.

5.1 Summary

The ICs are beginning to move to historical nano scale with <100nm lithography, 100 million transistors, requiring more than 10,000 I/Os on 20-50µm area array pitch and 200watts of power. There is a critical need for a microminiaturized, multi-function board to realize the complex electronic systems of the future. This system board has to support extremely high wiring density (>5000cm/cm^2) with 4-8 layers of 5µm wiring. The board must also support the assembly of large, fine pitch ICs and wafer level packages and be extremely reliable, preferably without expensive underfill materials.

To comply with these trends in microelectronics industry, this research was driven by above-mentioned board requirements for next generation microsystems. A novel manufacturing process has been demonstrated to yield large-area thin carbon-silicon carbide (C-SiC) based composite boards with potentially low cost and desired thermomechanical properties - ultra high modulus, Si-matched CTE and large-area

manufacturability. Using both FEM and experimental analysis, this work reports evaluation of this novel SiC-based ceramic composite board material for ultra-fine pitch solder-joint reliability without underfill and high-density wiring capabilities.

To assess thermomechanical reliability of assemblies on C-SiC boards, 2D FEM models were formed to simulate thermal cycling. A 200µm solder (Sn/Pb) pitch peripheral flip-chip of size 5mm x 5mm was modeled to show the effect of substrate CTE and modulus on the package reliability. This model was also used to calculate accumulated plastic strain to predict fatigue life (using Coffin-Manson equation) of the assemblies. Dielectric stresses, calculated from these models predicted thinner advanced (low CTE, high strength) dielectrics like BCB, PI and PPE more reliable than thick conventional dielectrics like epoxy. Actual test vehicles with flip-chip (200µm solder-pitch, Sn/Pb solder, 5mm x 5mm size) assembly without underfill were fabricated and subjected to thermal shock tests from -55°C to 125°C in liquid media. Experimental results showed good agreement with the FEM predictions. Test vehicles with thick (60µm) epoxy failed within 300-500 cycles due to dielectric cracking but the ones with thin (5-30µm) BCB and PPE survived >1000 cycles without any failure. These FE models were also used to predict the effect of solder-pitch, die size and solder material on the reliability of flip-chip assemblies.

A test vehicle having 20mm x 20mm flip-chip with lead-free solder (Sn0.7Cu) at 100µm pitch assembled on C-SiC without underfill was modeled and fabricated to evaluate C-SiC much more aggressively for thermomechanical reliability. FE models predicted good reliability even for such a large die at fine pitch. Experimental results of thermal shock testing from 0°C to 100°C in air confirmed FE results and the test vehicles

survived >1000 cycles without any failure. This work successfully demonstrated >1000 cycle reliability for 20mm x 20mm size flip-chip at 100µm solder pitch (assembled without underfill) for the first time.

High-density wiring capabilities of C-SiC were evaluated in terms of microvia reliability and via-pad misregistration. 2D axisymmetric model containing one microvia was modeled to assess microvia reliability in terms of via strains and dielectric stresses. FEM results predicted higher strains and hence, lower reliability for smaller diameter vias. Simulations also predicted that via strains with for C-SiC/BCB are less than for C-SiC/epoxy test vehicles. Two metal layer (metal-via-metal) test vehicles containing vias with diameters 50µm, 75µm, 100µm and 125µm were fabricated with BCB and subjected to thermal shock tests from -55°C to 125°C in air. All the vias survived >1200 thermal cycles showing excellent microvia reliability for all via diameters on C-SiC.

2D half-symmetry model was formed to simulate coating (curing) of different BCB layers. Warpage, as obtained from the models was used to calculate the curvature κ of the board. This curvature was used to calculate via-pad misregistration. Variation of misregistration with distance and film thickness was obtained from the models. Test vehicles having copper pads on C-SiC were fabricated and, board warpage and cu-pad displacement was measured after each BCB layer coating. Experimental results for C-SiC showed good agreement with FE predictions. Simulations also predicted that misregistration for FR-4 (24GPa) is ~5-6 times more than C-SiC (180GPa). FE results, when extrapolated, predicted that misregistration across a 400mm diagonal of a 300mm x 300mm board coated with four layers (8µm each) of BCB is ~96µm for FR-4 (24GPa), ~17µm for 180GPa C-SiC and ~7µm for 350GPa C-SiC. Therefore, 350 GPa C-SiC can

meet the stringent requirements of 20µm vias on 30µm capture pads while FR-4 may not be suitable even for 50µm vias on 100µm capture pads.

The proposed high-performance ceramic composite substrate material in combination with ultra low-loss dielectric showed the required attributes of Si-matched CTE and high modulus for ultra-fine pitch large die solder joint reliability, dielectric reliability and microvia reliability. C-SiC boards also exhibit low via-pad misregistration, making them suitable for building multilayered structures on a larger area with smaller via capture pads. In addition, the processability of these boards enables them to be manufactured in large area at low-cost. These boards have the potential to be the ideal candidate board materials for next-generation high-density packaging requirements.

5.2 Future Work

This work evaluated the thermomechanical reliability of flip-chip assemblies and high-wiring density capabilities of C-SiC board material. There are several other aspects of evaluation which can be used to present a more complete picture in order to make it more readily acceptable for use by microelectronics industry.

5.2.1 Planarization Techniques

An in-depth study for the assessment of planarization techniques (lamination, spin-coating etc.) may be helpful to decide about the best method to planarize C-SiC. Alternatively, ways of reducing porosity by the use of fillers in the preceramic polymer may also be helpful in reducing the roughness of C-SiC boards.

5.2.2 Mechanical Shock Testing

Mechanical shock and vibration testing data of flip-chip assemblies on C-SiC might be useful for portable electronics industry.

5.2.3 Electrical Characterization

Electrical characterization of C-SiC board material in terms of dielectric constant, dielectric loss, resistivity measurements etc. might be helpful for its use in integrating RF and high-speed digital components. If the boards are too conductive (because of carbon fibers) for these requirements, use of insulating fibers to lower the conductivity may be evaluated.

5.2.4 Machinability

Drilling capability would enable C-SiC board usage and build-up on both sides. Feasibility study of mechanical drilling, electric discharge drilling, laser drilling etc. might be useful. Reliability modeling of through holes in C-SiC may also be evaluated.

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